HPEC Poster Session Abstract

Performance Estimates of a STAP Benchmark on the IBM Cell Processor

Mr. Luke Cico (lcico@mc.com), (978) 967-1679 (principal author/presenter)
Mr. Jon Greene (jgreene@mc.com)
Dr. Robert Cooper (rcooper@mc.com)
Mercury Computer Systems
199 Riverneck Rd
Chelmsford, MA 01824-2920
All authors are citizens of the United States of America

Categories:

- Performance Modeling and Simulation for Benchmarking Embedded Systems
- Algorithm Mappings to High Performance Architectures

Advances in COTS embedded computing technologies have yielded impressive gains in computational throughput over the past 5-10 years. Adaptive sensor array systems utilizing real-time teraflop class machines are in wide deployment today. Gains in processor density have generally been achieved by steady improvements in semiconductor optical lithographic processes along with less frequent innovations in processor chip architectures. It is likely that the real-time embedded community is entering an era where processor architectural innovations will be bearing most of the burden for producing processing density gains as lithographic processes approach fundamental physical limitations. More and more 'systems on a chip' are emerging to address these trends. An exciting example of this technology trend is IBM's new Cell architecture which offers 200 GFLOPs of SIMD compute power on multiple VMX-like processors interconnected with a 200GB/s internal fabric.

This poster explores the application of a computationally intensive adaptive nulling problem on the Cell architecture. Expectations based on initial analysis of this architecture are that computational throughput gains of 10X are possible and, furthermore, that throughput per watt will improve by several factors over what is achieved with the current generation of high performance floating point general purpose programmable processors.

The reference application is the RT_STAP benchmark developed by MITRE Corporation and serves as a fair representation of the processing requirements of a STAP mode for a modern radar system. The benchmark represents a processing mode with 22 spatial channels sampled at 5MHz and performs 3rd order post doppler adaptive nulling along with pulse compression and doppler filtering operations. The mode represents a computational throughput of 39 GFLOPS for all stages of processing. This poster will present an analysis of a mapping of the RT_STAP benchmark to the Cell architecture. The analysis will examine the gains in processor throughput and throughput per watt relative to current technology.