



# Pipelined Data Path for an IEEE-754 64-Bit Floating-Point Jacobi Solver

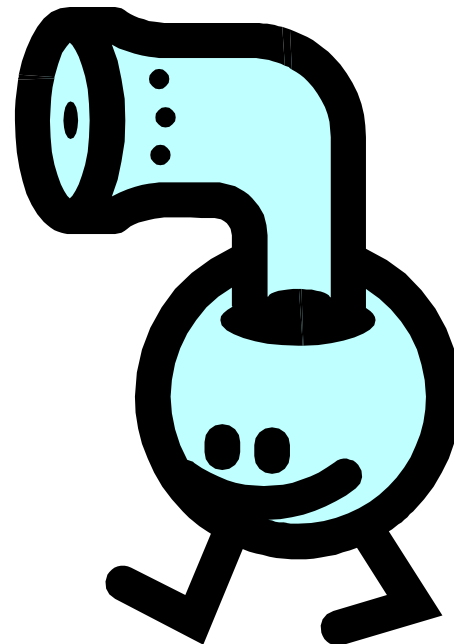
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**USC Viterbi**  
School of Engineering

- **Iterative Methods**
- **Jacobi Data Path Design**
- **Experiments**
- **Related Work**
- **Acknowledgments**
- **Questions**



- **Approach**

- manipulate equation to look like

$$\mathbf{x} = f(\mathbf{x}) \quad [1]$$

- iteratively compute  $\delta + 1^{th}$  value as

$$\mathbf{x}^{(\delta+1)} \Leftarrow f(\mathbf{x}^{(\delta)}) \quad [2]$$

- **Example: scalar quadratic equation with known solution**

$$0 = (x + 2)(x - 5)$$

$$0 = x^2 - 3x - 10$$

$$x^2 = 3x + 10$$

$$x = \sqrt{3x + 10} \quad ([1])$$

$$x^{(\delta+1)} \Leftarrow \sqrt{3x^{(\delta)} + 10} \quad ([2])$$

$\delta$	$x^{(\delta)}$	$\sqrt{3x^{(\delta)} + 10}$
0	1.000	3.606
1	3.606	4.563
2	4.563	4.867
3	4.867	4.960
4	4.960	4.988
5	4.988	4.996
6	4.996	4.999
7	4.999	5.000

- **Jacobi iterative method solves  $A\mathbf{x} = \mathbf{b}$** 
  - $n \times n$  diagonally dominant real-valued matrix,  $A$
  - the unknown real-valued  $n$ -vector,  $\mathbf{x}$
  - constant real-valued  $n$ -vector,  $\mathbf{b}$
- **Derivation: plug  $A = L + U + D$  into  $A\mathbf{x} = \mathbf{b} \rightarrow (L + U + D)\mathbf{x} = \mathbf{b}$** 
  - lower triangular matrix,  $L = \{a_{ij} \mid i > j \text{ else } 0\}$
  - upper triangular matrix,  $U = \{a_{ij} \mid i < j \text{ else } 0\}$
  - diagonal matrix,  $D = \{a_{ij} \mid i = j \text{ else } 0\}$

**vector form**

$$\mathbf{x}^{(\delta+1)} \Leftarrow D^{-1} [\mathbf{b} - (L + U)\mathbf{x}^{(\delta)}]$$

**point form**

$$x_i^{(\delta+1)} \Leftarrow \frac{1}{a_{ii}} \left[ b_i - \sum_{j=1, j \neq i}^{j=n} a_{ij} x_j^{(\delta)} \right]$$

# Jacobi Iterative Method

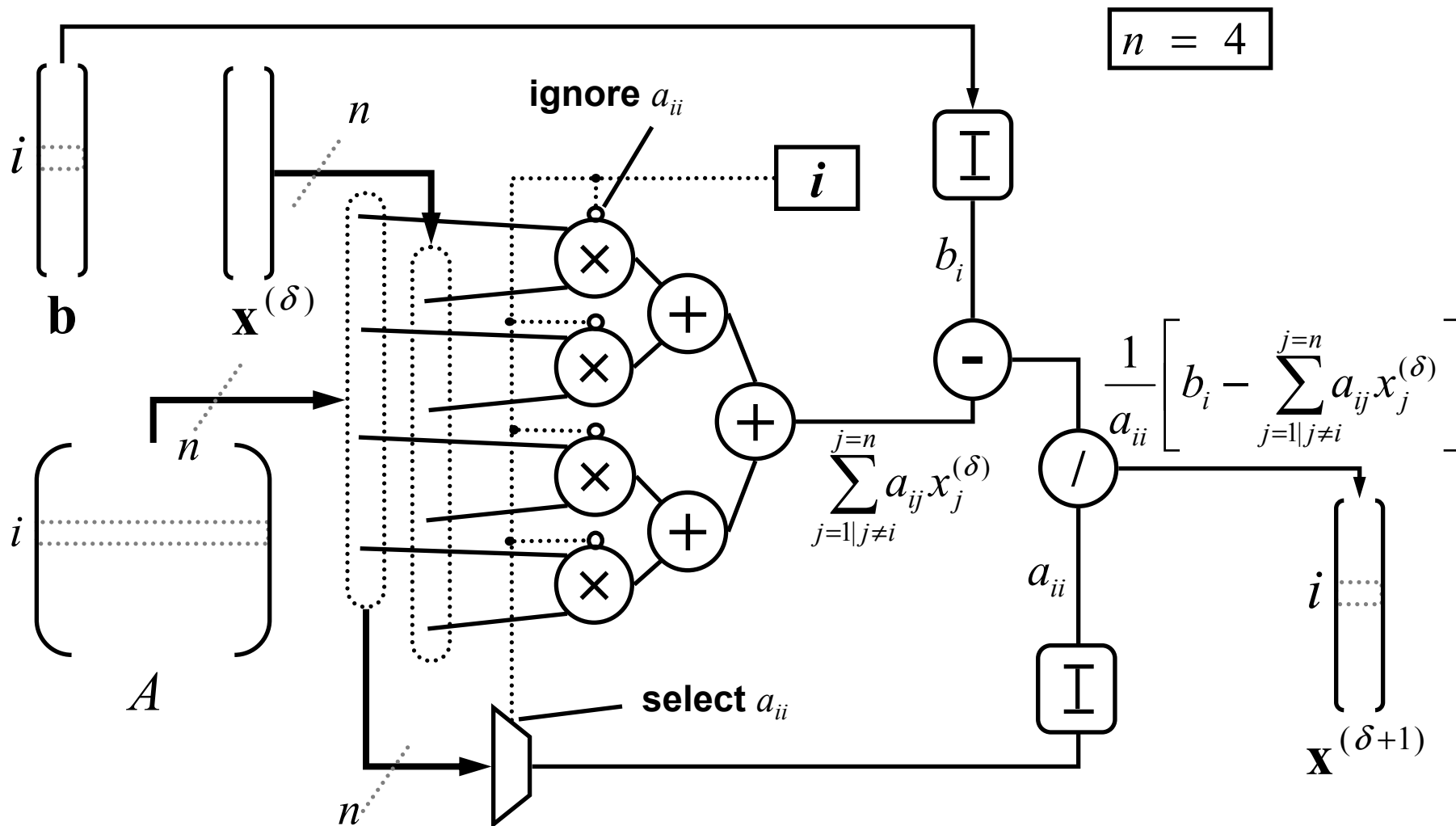
- Example:  $2 \times 2$  linear equation with known solution

$$A\mathbf{x} = \mathbf{b}$$

$$\begin{bmatrix} 3 & 2 \\ 1 & 4 \end{bmatrix} \begin{bmatrix} 2 \\ 3 \end{bmatrix} = \begin{bmatrix} 12 \\ 14 \end{bmatrix}$$

$\delta$	$(\mathbf{x}^{(\delta)})^T$		$(D^{-1}[\mathbf{b} - (L+U)\mathbf{x}^{(\delta)}])^T$	
0	1.000	1.000	3.333	3.250
1	3.333	3.250	1.833	2.667
2	1.833	2.667	2.222	3.042
3	2.222	3.042	1.972	2.944
4	1.972	2.944	2.037	3.007
5	2.037	3.007	1.995	2.991
6	1.995	2.991	2.006	3.001
7	2.006	3.001	1.999	2.998
8	1.999	2.998	2.001	3.000
9	2.001	3.000	2.000	3.000

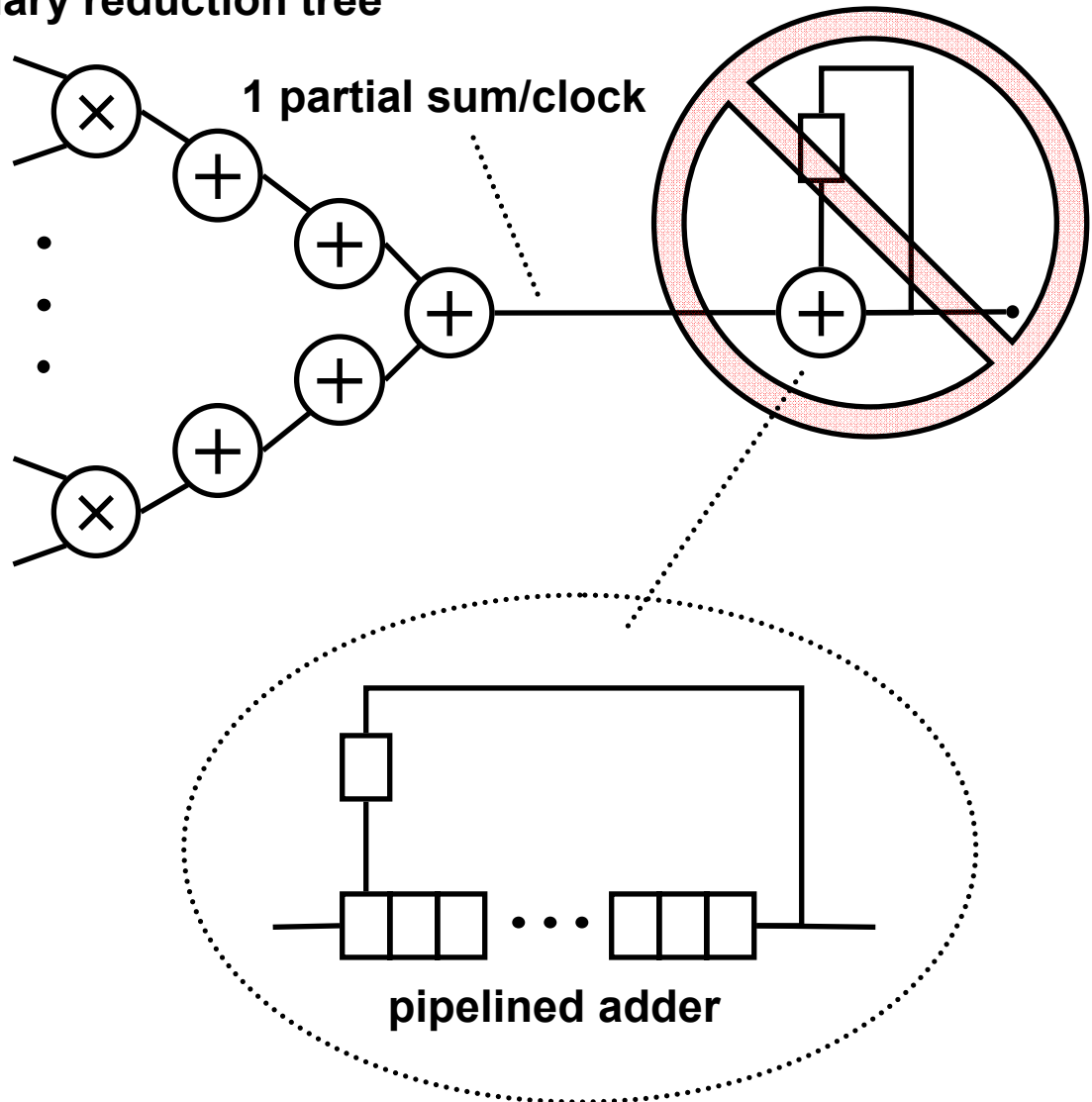
# Idealized Jacobi Circuit



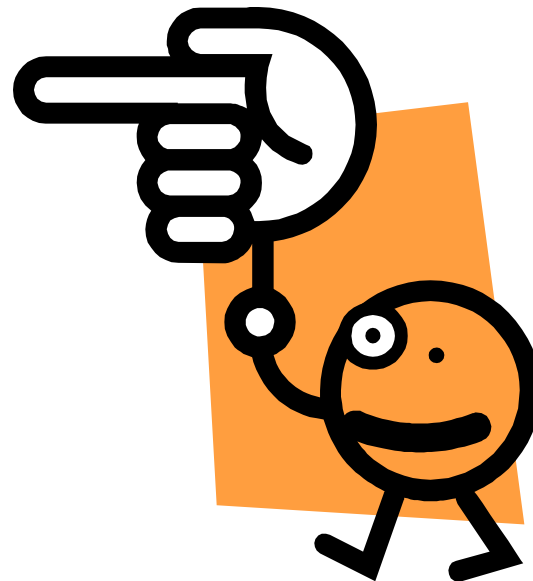
# Design Issues

- **Pipelined FPU's**
  - many stages
  - higher frequency
- **Scalability**
- **Reduction**
  - adder “loop” fails
  - pipeline latency
- **Serialized**
  - division last
  - very costly

binary reduction tree



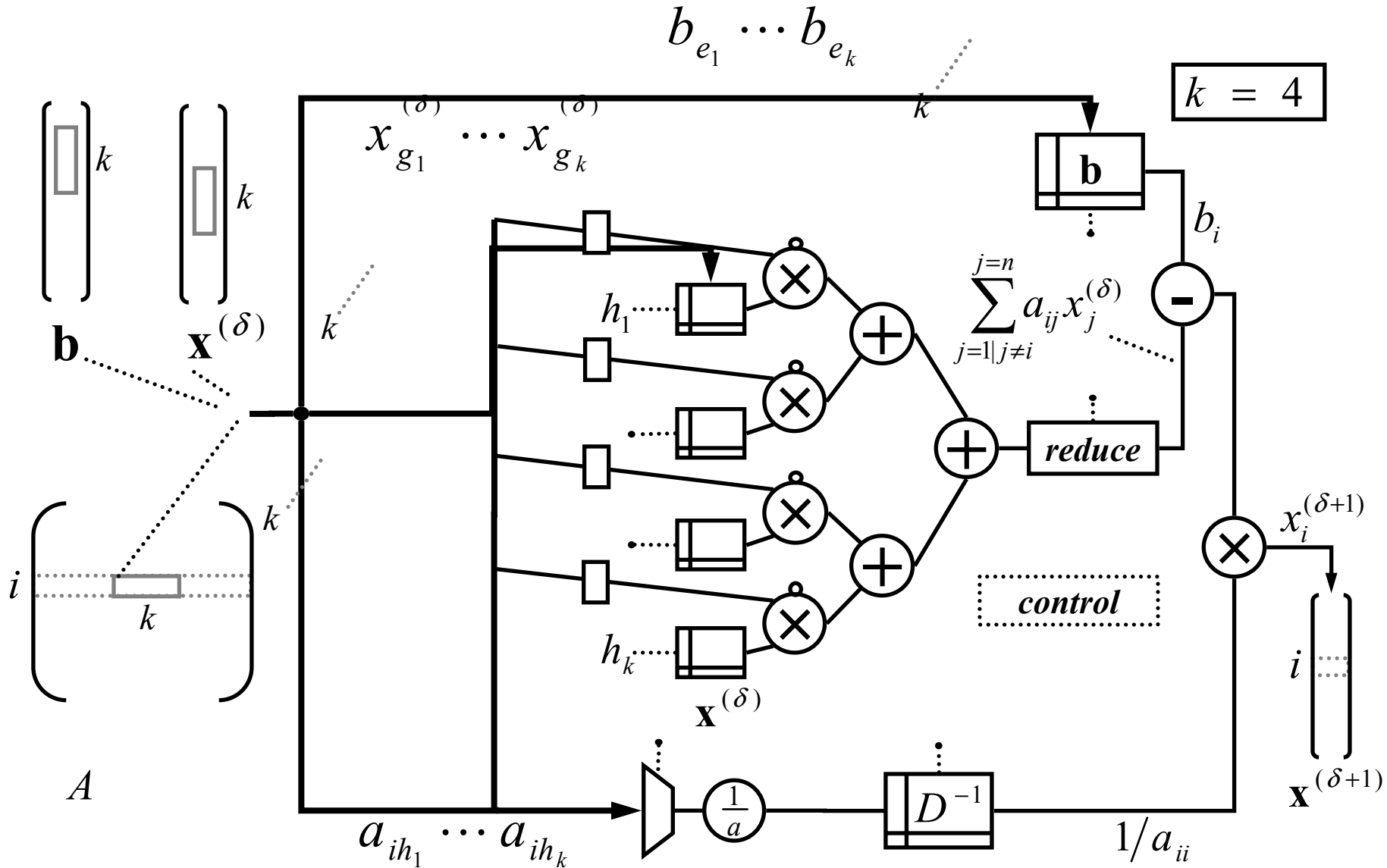
- **Pipelined  $k$ -vector data path**
  - deeply pipelined FPU's
  - input one  $k$ -vector per clock
- **Multiplexed inputs**
  - store  $x, b$  in on-chip BRAM
- **Reduction circuit**
  - accumulates  $n/k$  partial sums
  - no stalls, no buffer overflow
- **Hidden divider latency**
  - store  $D^{-1}$  in on-chip BRAM
- **Flexible (dense or sparse)**





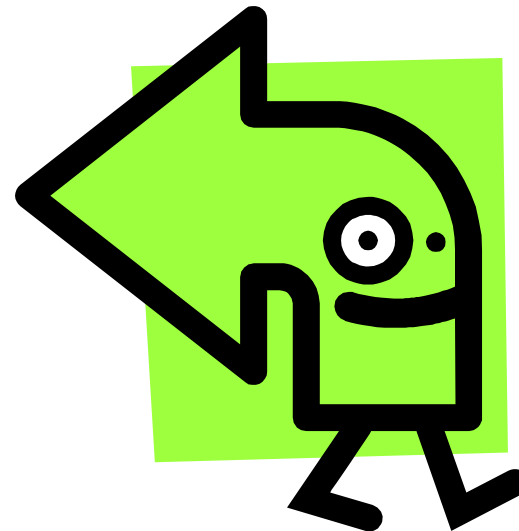


# Dense Matrix



# Sparse Matrix?

- **Same pipelined data path**
- **Compressed sparse row (CSR) format**
- **Minor modifications**
  - **input column (col)**
  - **input row pointer (ptr)**
  - **controller mods**



# Compressed Sparse Row Format

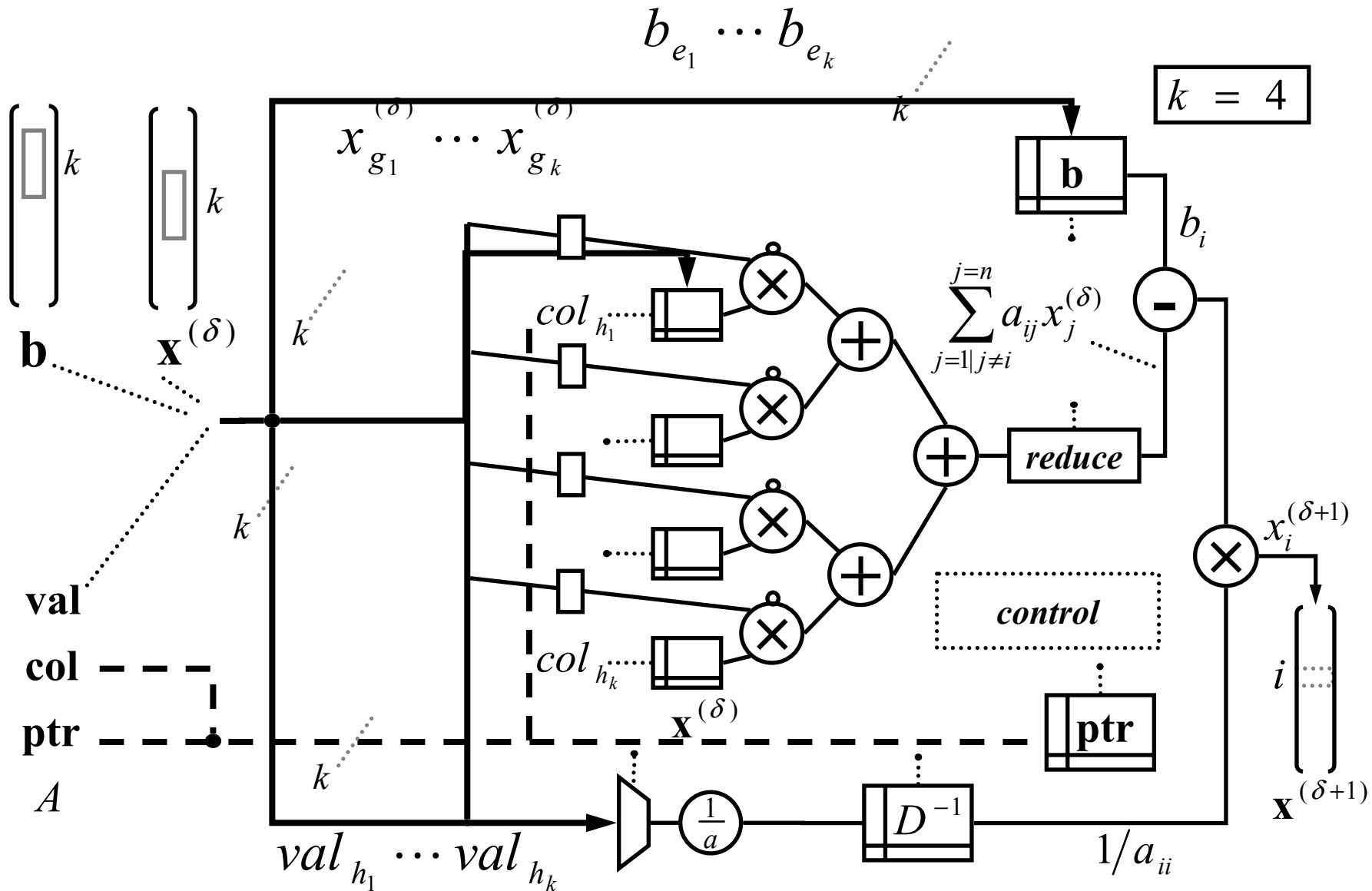
- Mostly 0's ( $nnz$  non-zeros)
- Use three vectors
  - val: non-zero values (row wise)
    - $|val| = nnz$
  - col: column index of each non-zero
    - $|col| = nnz$
  - ptr: index in val where row  $i$  starts
    - $|ptr| = n + 1$
    - by convention,  $ptr_{n+1} = nnz + 1$
- Number of non-zeros/row
  - calculated as  $len_i = ptr_{i+1} - ptr_i$

- Example for  $n = 4$

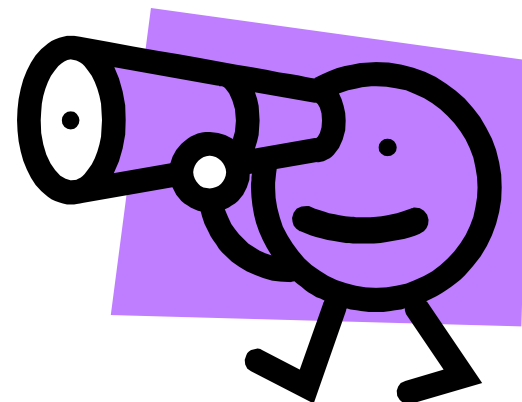
$$A_{n \times n} = \begin{bmatrix} 5 & 0 & 0 & 2 \\ 0 & 8 & 0 & 0 \\ 1 & 0 & 6 & 0 \\ 0 & 0 & 0 & 3 \end{bmatrix}$$

$i$	1	2	3	4	5	6
val	5	2	8	1	6	3
col	1	4	2	1	3	4
ptr	1	3	4	6	7	
len	2	1	2	1		

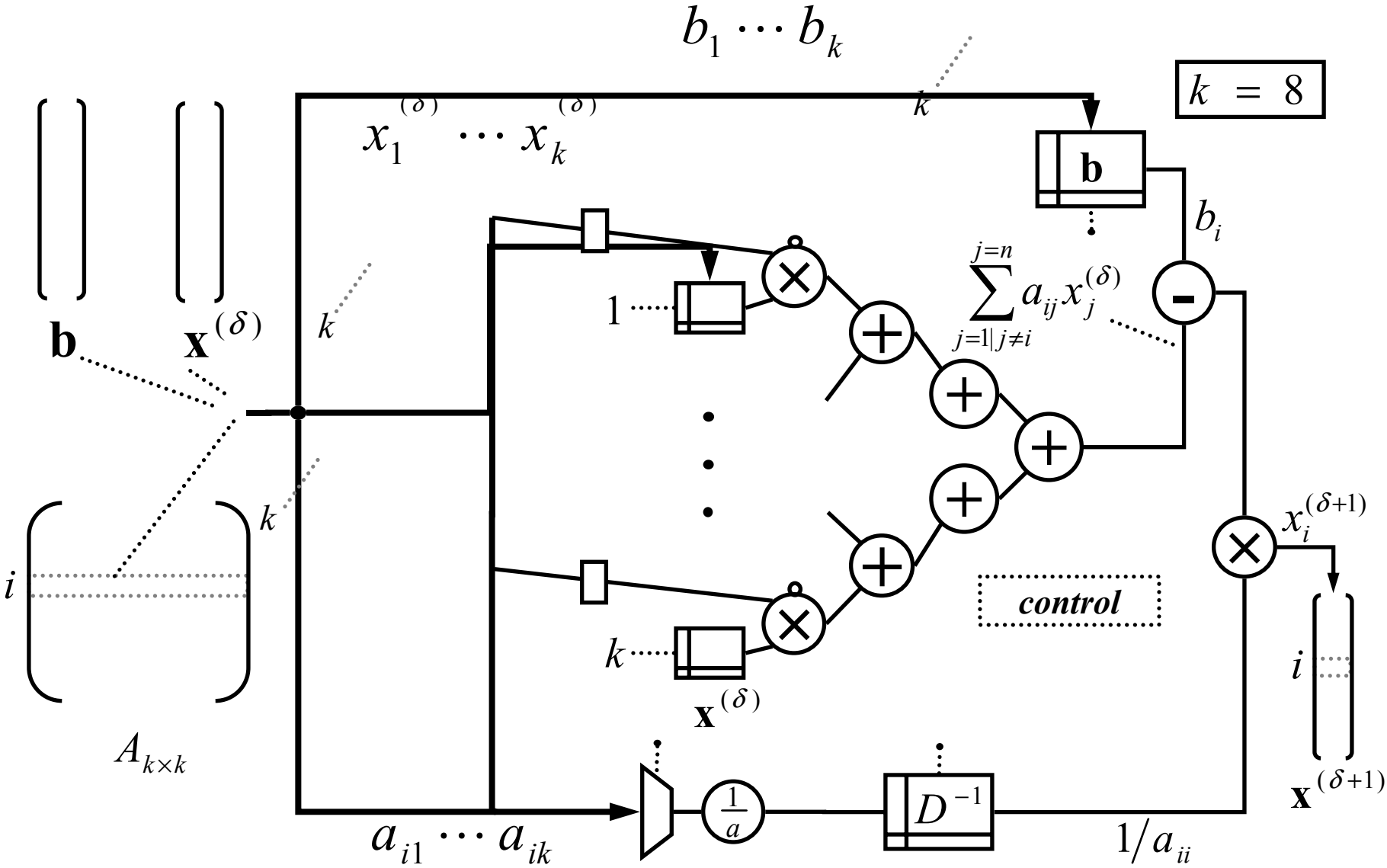
# Sparse Matrix!



- **Tools**
  - VHDL
  - Xilinx ISE 6.3.03i
  - ModelSim XE II 5.8c
  - Synplify Pro 8.1
- **64-Bit IEEE-754 floating-point IP cores**
  - adder
  - multiplier
  - divider
- **Targets**
  - Virtex-II Pro XC2VP70-6
  - Virtex-II Pro XC2VP100-6



# Data Path



# Experimental Results

## IP Core Post-PAR Statistics

IP core	latency [cycles]	$f_{\max}$ [MHz]	area [slices]
adder	14	170	1078
multiplier	10	170	935
divider	58	140	3015

## Jacobi Data Path Post-PAR Statistics

FPGA device	k	I/O pins	latency [cycles]	$f_{\max}$ [MHz]	area [slices]
XC2VP70	8	581	52	103	20188
XC2VP100	8	581	52	107	20527

## Floating-Point IP Cores

G. Govindu, R. Scrofano, and V.K. Prasanna, “A Library of Parameterizable Floating-Point Cores for FPGAs and their Application to Scientific Computing,” *International Conference on Engineering Reconfigurable Systems and Algorithms (ERSA'05)*

## Reduction Circuits

G.R. Morris, L. Zhuo, and V.K. Prasanna, “High-Performance FPGA-Based General Reduction Methods,” *Symposium on Field-Programmable Custom Computing Machines (FCCM'05)*

## Complete Jacobi Design (to appear)

G.R. Morris and V.K. Prasanna, “An FPGA-Based Floating-Point Jacobi Iterative Solver,” *International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN'05)*

## Conjugate Gradient (manuscript in preparation)

G.R. Morris and V.K. Prasanna, “Accelerating Conjugate Gradient on an FPGA-Augmented Reconfigurable Computer”



# Acknowledgments

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