Rapid Prototyping of a Real-Time Range Compression Processor

M. Vai, T. Anderson, A. Horst, R. Gallagher, L. Retherford, T. Emberley, P. Jackson, C. Chan, C. Rader, H. Nguyen, and P. Monticciolo

Massachusetts Institute of Technology
Lincoln Laboratory

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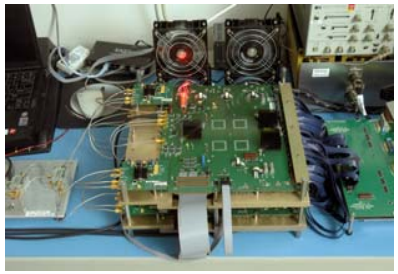
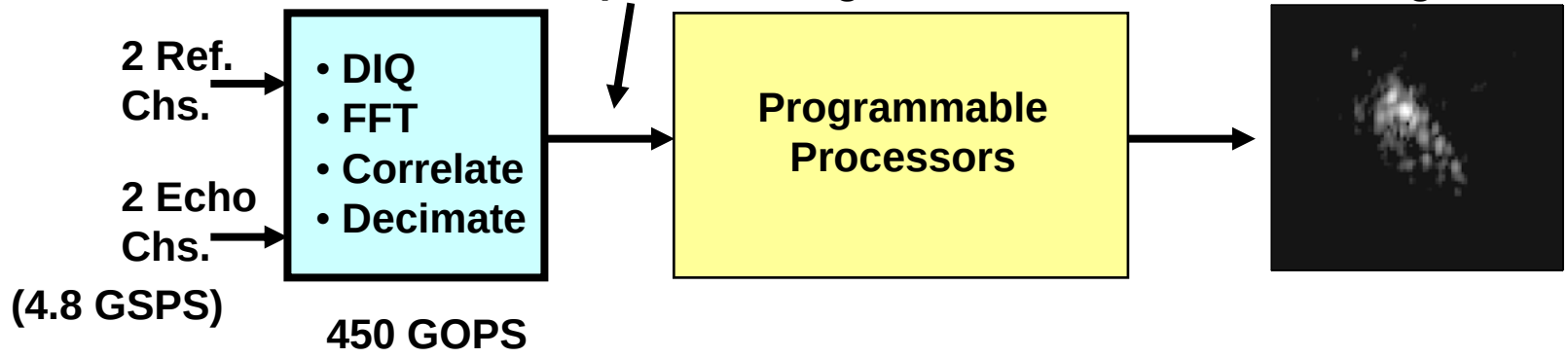
Real-Time Processor Highlights





Chip Level

- 6 Xilinx Virtex II 8000 FPGAs
- 30,000 VHDL lines (FPGA design)
- 2,000 Matlab lines (Floating point, fixed point, bit-true models)
- 150 MHz FPGA operation
- 450 GOPS (3.5 GOPS/W)

System Level

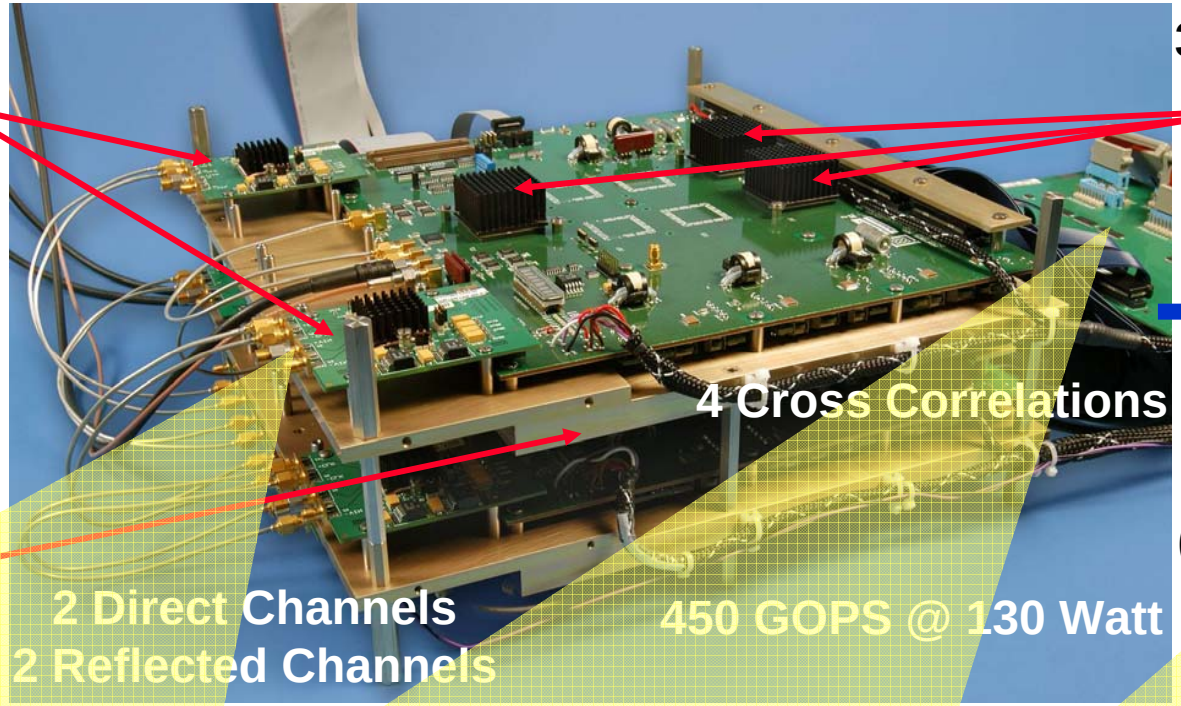
- 2 high-performance main boards
- 4 1.2 GBPS ADC (Max 108) daughter cards
- 4 real-time correlation outputs
- 13 GBPS I/O
- 4,000 C/Matlab lines (API)
- 1 year development time

SYCO Real-Time Processor Highlights

*A Systolic FFT Architecture for Real-Time FPGA Systems, HPEC 2004

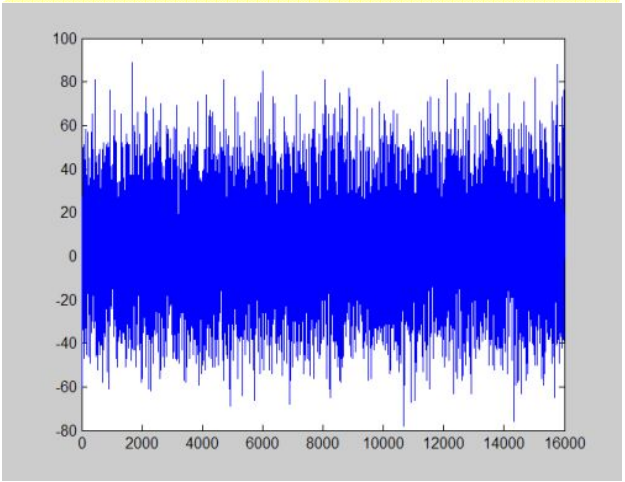
2 Analog-to-Digital Converters (1.2 GSPS) Per Board

3 High-Performance FPGAs Per Board

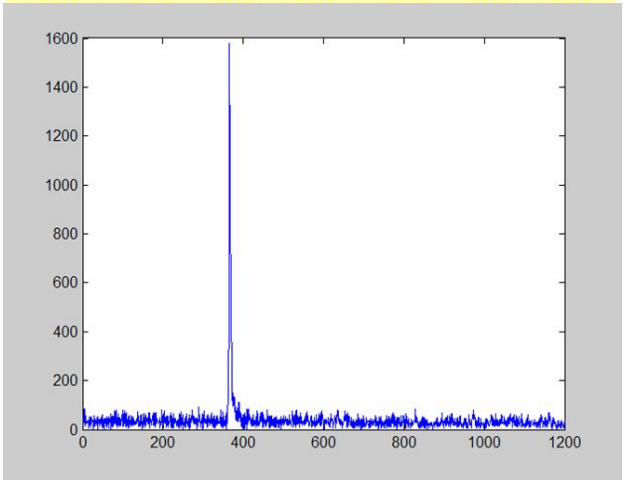


2-Board Stack Assembly Designed for Airborne Operations

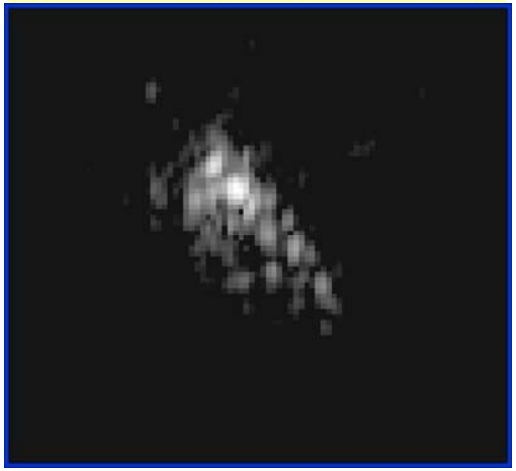
Backprojection (pMatlab on LL Grid)



Direct and Reflected Signals



Cross Correlation Results



SAR Image

To Probe Further

- **Systolic FFT architecture:**
  - **P. Jackson et al, "A Systolic FFT Architecture for Real-Time FPGA Systems," HPEC 2004**
- **Ultra-Long FFT's:**
  - **H. Kim et al, "Advanced Hardware and Software Technologies for Ultra-long FFT's," HPEC 2005**
- **Another rapid prototyping example:**
  - **H. Nguyen et al, "High-Performance FPGA-Based QR Decomposition," HPEC 2005**