

Interface Techniques for Microprocessors Embedded Within FPGAs

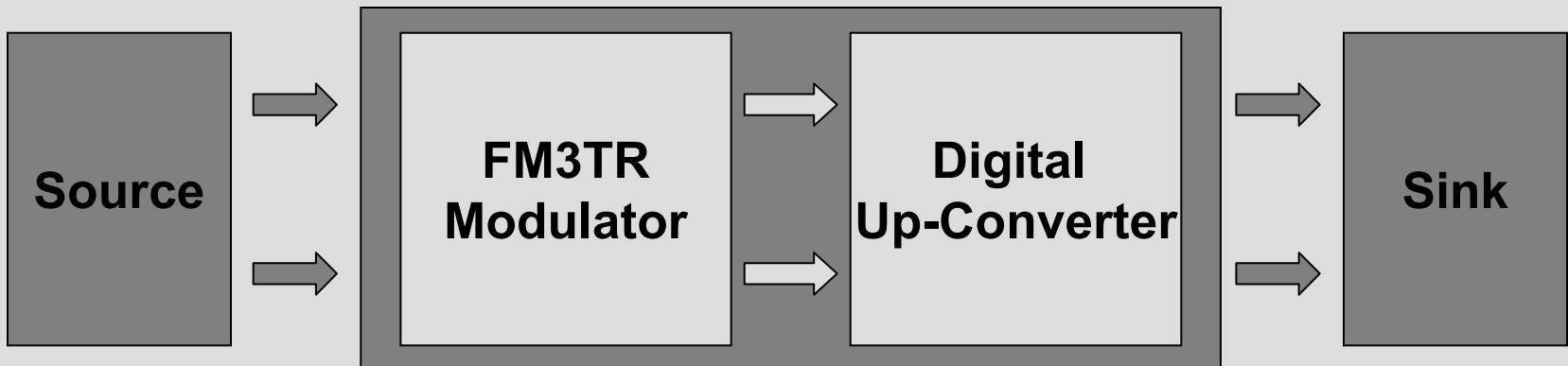
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- Xilinx's Virtex-II Pro FPGA integrates embedded PowerPC processors and reconfigurable logic on a single chip
- We map a Software Defined Radio application to a Virtex-II Pro FPGA
- Application serves as a vehicle to investigate the following:
 - PowerPC Processor Local Bus (PLB) Interface
 - PowerPC On-Chip Memory (OCM) Interface
 - PowerPC Cache
- The types of data that are communicated over these interfaces effect an application's performance



FM3TR Application Overview



- Use multiple implementations of the FM3TR Application
- Each implementation uses a unique memory configuration

- Memory
 - On Chip Memory (OCM)
 - Data/Instruction-Side
 - Processor Local Bus (PLB)
 - Data/Instruction-Side

- Data
 - Application Data
 - Input/Output
 - Program Data
 - Stack/Heap
 - Instruction Data
 - PPC Instructions

Results

Implementation	Instruction Location	Stack/Heap	Application Data	I-Cache	D-Cache	Total Cycles
1.a	ISOCM	PLB BRAM	DSOCM	DISABLED	N/A	28394
1.b	ISOCM	DSOCM	DSOCM	N/A	N/A	21286
1.c	ISOCM	PLB BRAM	DSOCM	ENABLED	N/A	21278
2.a	ISOCM	DSOCM	PLB BRAM	N/A	ENABLED	26182
2.b	ISOCM	PLB BRAM	PLB BRAM	N/A	ENABLED	36146
3.a	PLB BRAM	DSOCM	PLB BRAM	DISABLED	DISABLED	53525
3.b	PLB BRAM	DSOCM	PLB BRAM	DISABLED	ENABLED	55961
3.c	PLB BRAM	DSOCM	PLB BRAM	ENABLED	DISABLED	24178
3.d	PLB BRAM	DSOCM	PLB BRAM	ENABLED	ENABLED	24261
4.a	ISOCM	DSOCM	OPB BRAM	DISABLED	DISABLED	37004
4.b	PLB BRAM	DSOCM	OPB BRAM	DISABLED	DISABLED	64129
4.c	PLB BRAM	DSOCM	OPB BRAM	ENABLED	DISABLED	38078

- Appropriate interface selection can improve the performance of an application
- The OCM and PLB interfaces deliver comparable performance
- The OPB delivers performance that is comparable to the PLB in specific scenarios
- Data that exhibits certain attributes should be communicated over one interface versus another
 - Spatial Locality
 - Temporal Locality
- Use of the PowerPC's cache can hurt an application's performance