Super-pipelined CORDIC Unit

With Application to Power System Analysis

Presenter: Prawat Nagvajara

Authors: Michael Fitzharris, Jeremy Johnson, Servesh Tiwari, Prawat Nagvajara

Drexel University

This work is supported by the United States Department of Energy (DOE) under Grant No. CH11171

Synopsis

- In applications such as power system analysis (e.g., the load flow computation) FPGA hardware to accelerate sine and cosine functions offers a cost-effective solution
- In these applications the host can stream a set of angles to the hardware which streams back the sine and cosine
- CORDIC (COordinate Rotation DIgital Computer) Pipeline structure allows maximal clock speed
- With host/FPGA interconnection, e.g., PCIX, FPGA implementation can provide an order of magnitude speedup over general-purpose personal computer

Load Flow Computation

Power flow equations

$$P_i = \sum_{k=1}^{n} |V_i|\,|V_k|\,[G_{ik}\cos(\theta_i - \theta_k) + B_{ik}\sin(\theta_i - \theta_k)] \qquad i = 1, 2, 3, \ldots, n$$

$$Q_i = \sum_{k=1}^{n} |V_i|\,|V_k|\,[G_{ik}\sin(\theta_i - \theta_k) - B_{ik}\cos(\theta_i - \theta_k)] \qquad i = 1, 2, 3, \ldots, n$$

System	Branches	NNZ YBUS	NNZ Jacobian	Jacobian Size
1648 Bus	2,602	6,680	21,196	2,982
7917 Bus	13,014	32,211	105,522	14,508
10279 Bus	14,571	37,755	134,621	19,285
26829 Bus	38,238	99,225	351,200	50,092

CORDIC Example

$$\begin{bmatrix} x' \\ y' \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} = \cos(\theta) \begin{bmatrix} 1 & \tan(\theta) \\ -\tan(\theta) & 1 \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix}$$

Desired angle 28 deg.

Initialization

x = 1

y = 0

α= 0 deg.

First Rotation

x_{new} = x - y/1 = 1

y_{new} = x/1 + y = 1

α= 45 deg.

Second Rotation

x_{new} = x + y/2 = 1.5

y_{new} = -x/2 + y = 0.5

arctan ½ = 26.5651 deg.

α= 18.44 deg.

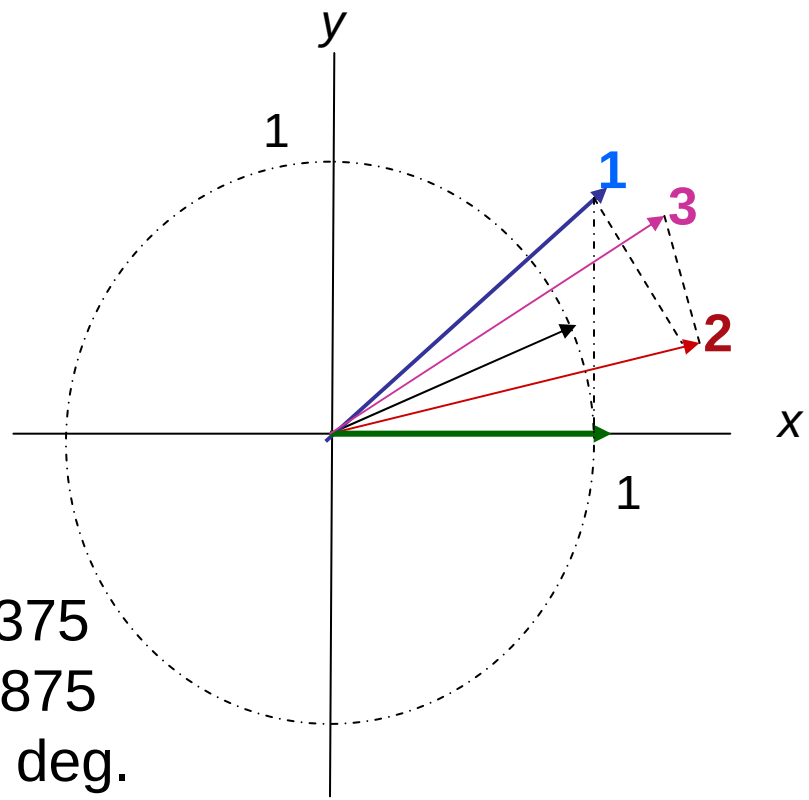
Third Rotation

x_{new} = x - y/4 = 1.375

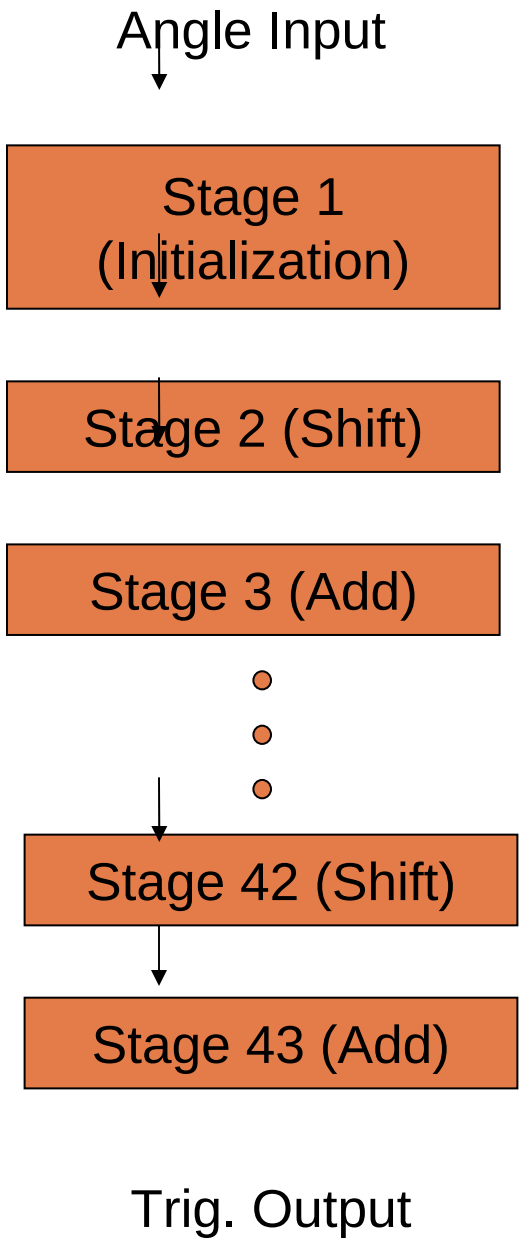
y_{new} = x/4 + y = 0.875

arctan ¼ = 14.0363 deg.

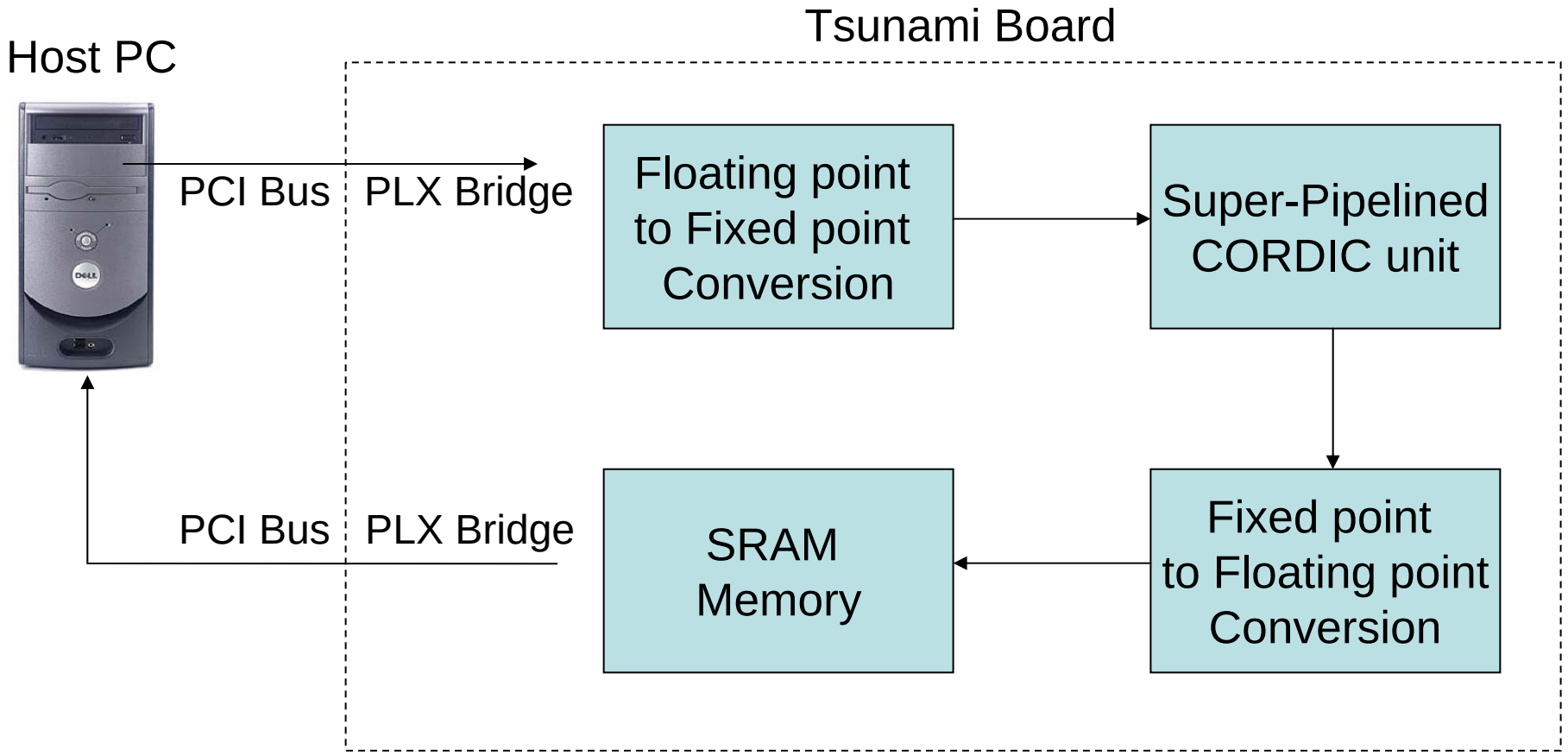
α= 32.47 deg



Super-Pipelined CORDIC



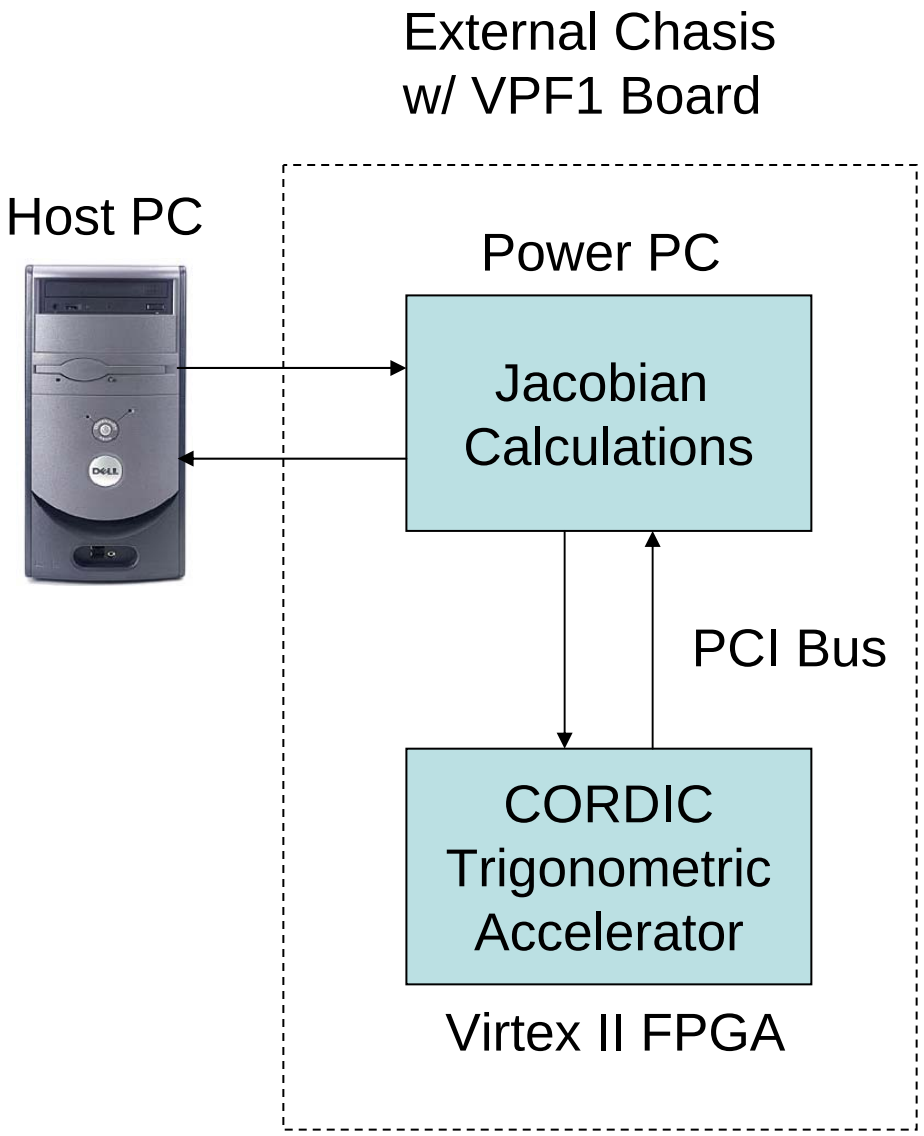
Current Implementation



- DMA transfers occur between the host PC and FPGA in both directions
- Software running on the host PC handles all other calculations

Future Implementation

- The benefit of the VPF1 board are the dual external Power PC processors which are well equipped to handle the Jacobian construction.
- The CORDIC Processor will be implemented on either of the two on-board FPGAs.
- A 125 MHz PCI bus will be used for the communication, which can reach its full frequency potential due to the FPGA's priority.



Projected Performance