# Rapid Prototyping of a Real-Time Range Compression Processor

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## Introduction

This paper describes the rapid prototyping of a high-performance real-time processor (RTP) for a sensor application. This prototyping project is significant in two aspects. First, the use of FPGA technology in the development of a high-bandwidth, high-throughput, real-time system was demonstrated. Also, after determining that the use of COTS (commercially off-the-shelf) FPGA boards would present a high risk to the project schedule, a custom FPGA-based processor board, previously developed at Lincoln Laboratory for a different functionality, was quickly adopted as the prototyping platform for this RTP. Despite the need to go through a PCB (printed circuit board) modification and manufacturing cycle, the development of this RTP was successfully completed in one year.

## Functionality

The RTP input consists of 2 reference and 2 echo channels with a data rate of 1.2 GSPS per channel. The real input data are converted into a complex format and cross-correlated to produce 4 correlation outputs (i.e., range compression).

## Implementation Platform

An analysis was performed to match up the computational and communication requirements with COTS FPGA boards. While COTS boards may have adequate computational resources (i.e., 2 to 3 large FPGAs), they are limited by insufficient data communication bandwidth and power supply. Although a design could have been created to circumvent the COTS limitations, we decided that the COTS approach was posting an unnecessary high risk on the project schedule. In fact, the result of this analysis showed that a custom FPGA board was warranted to accommodate the high computational and communication requirements.

The development of a custom board was ruled out due to schedule constraints. Instead, a different approach was pursued, which was to adopt an MIT/LL FPGA-based wideband adaptive beamforming processor board, hereinafter referred to as the BF board, as the implementation platform for this RTP prototype [1].

## Prototyping

Figure 1 shows a picture of the RTP prototype, which contains 2 BF boards integrated with 4 1.2 GSPS ADC (Max 108) daughter cards to compute 4 real-time correlation outputs. The BF boards were enhanced by incorporating high-speed demultiplexer circuits to match the ADC output data rate (1.2 GSPS) with the FPGA interface (300 MSPS). Both FPGAs and custom VLSI chips were employed in the original BF board [1]. In this RTP prototype, the VLSI chip sites were not populated since the entire application was implemented in the FPGAs. A total of 6 Xilinx Virtex II 8000 FPGAs clocked at 150 MHz were used to perform the cross correlations. The RTP has a throughput of 450 GOPS with a power efficiency of 3.5 GOPS/W.

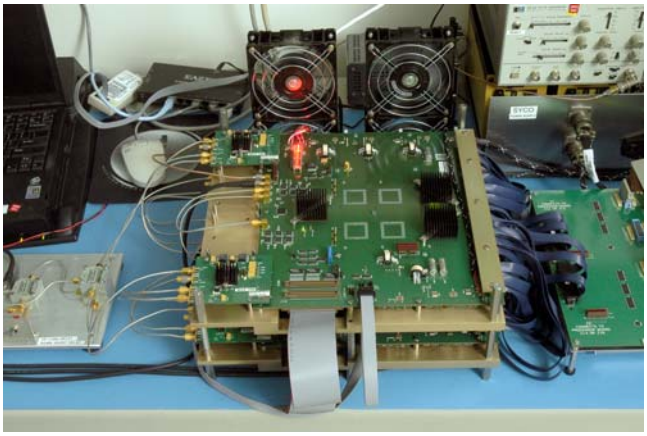

**Figure 1: RTP prototype**

Figure 2 illustrates the correlation processing between one reference channel and one echo channel. The objective of this architecture is to perform a correlation between 32K sample segments from these two channels, which would normally require the use of 32K-point FFTs. A segmented correlation scheme was devised to calculate only the required 4K lags from the correlation, which reduced the size of the FFT from 32K to 8K. An additional benefit of this segmented correlation scheme is that it allows the use of different correlation lengths to improve SNR (signal-to-noise ratio). The implementation utilized block floating-

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point computations. The word sizes at different stages were chosen carefully to provide the precision required by the applications.

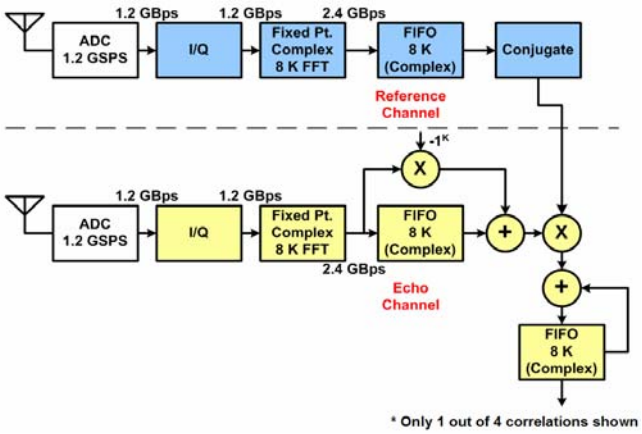


**Figure 2: Cross-correlation between a reference channel and an echo channel**

The 8K-point FFT in Figure 2 is an innovative systolic implementation, which uses FIFOs (first-in-first-out buffers) and switches to manipulate the data flow so that the data are processed by the butterflies with the right coefficients at the right time [2]. This design has a high degree of regularity and uses mostly local communication, which are both desired features for an FPGA implementation. Another important feature of this FFT design is that it is self-contained within the FPGA and does not require any off-FPGA memory to support its operation.

## Summary

In summary, the adoption of a custom FPGA board into a rapid prototyping platform for a different functionality was demonstrated. The benefits of adopting existing processor boards for the RTP were numerous. The material cost was significantly reduced from a similar COTS implementation. The BF board had an airborne form factor and provided adequate power rating and communication bandwidth to meet RTP requirements. In the future, the BF board can be redesigned to become a fully customized board (e.g., a board with the VLSI chips removed). The FPGA designs, without the need of any COTS specific interface, will be fully portable and allow an easy IP (intellectual property) transfer.

## References

[1] S. Leeper, R. Haney, H. Nguyen, and M. Vai, “FGPA beamforming in a wideband airborne radar system,” 7th Annual High Performance Embedded Computing Workshop, 22-25 September 2003.

[2] P. Jackson, C. Chan, C. Rader, J. Scalera, and M. Vai, “A systolic FFT architecture for real time FPGA systems,” 8th Annual High Performance Embedded Computing Workshop, 28-30 September 2004.