Real-time FPGA implementation of adaptive beamforming using QR decomposition

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Introduction

Increasing use of the radio spectrum in both the communication and military frequency bands is expected to result in increased interference, which must be coped with through improved design of antennas, receivers and processing systems. In the communication world, increasing use of antennas in built-up areas introduces multi-path effects and inter-system interference. In the military case the availability of low cost technology is expected to result in a proliferation of jamming systems.

Phased array antennas and adaptive beamforming (ABF) offer the potential to overcome many of the interference problems encountered, by reducing the antenna's sensitivity in the direction of the interference source, through modification of the relative phase and gain of the array elements.

Processing systems are therefore required that can provide real-time ABF. A PowerPC based solution was considered but found unsuitable due to speed and size constraints. FPGAs were identified as a suitable processing technology for these systems, as they could meet the speed and size requirements. FPGA cores for the required processing functions were subsequently developed.

Real-time adaptive beamforming

Many sensor systems, such as radar, require real-time processing of all data samples. This data can however be broken into distinct processing intervals, which define the available time in which all processing must be completed to maintain real-time operation. In the ABF case the adaptive weights, which define the phase and gain of each array element, need to be applied to the data from which they were calculated, to maximize the effectiveness of interference rejection. This requires the storage of data samples while ABF weight calculation is undertaken, introducing data latency into the system.

ABF weights can be calculated in the conventional covariance domain or the data domain via QR decomposition [1], which has been shown to be more suitable for FPGA implementation and more robust to reduced numerical precision, as a matrix inversion is not required. This results in a processing system as illustrated in Figure 1. This system utilizes a number of key FPGA cores: a QR decomposition core [2]; floating-point multipliers, dividers and adders [3]; a memory interface to create a FIFO using external memory; high speed serial FPGA interconnection; digital receiver.

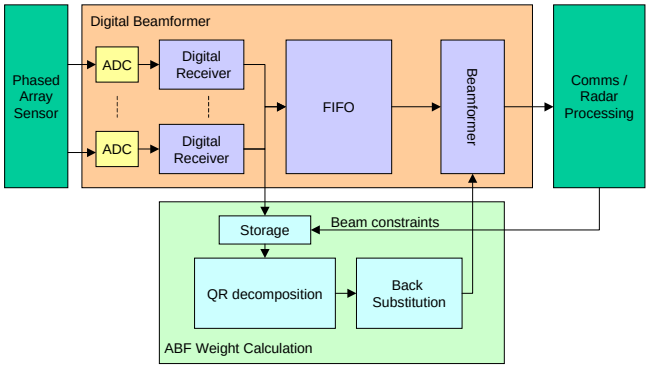

Figure 1: ABF system architecture

ABF weight calculation using QR decomposition

QR decomposition is a method for solving a set of simultaneous equations, for unknown weights, which define the beam shape. The solution that minimizes the received power is to set all of the weights to zero. To prevent this occurring, an additional gain constraint is required, which defines the required beam pointing direction. If the number of equations equals the number of array elements then a exact solution can be found, if more equations are available a minimum error solution will be determined.

The QR core employs Givens rotation [4] to convert the input data into an upper triangular matrix, which can be solved for the weights via back substitution. The Givens rotation employs two processing units called vectorise and rotate cells, as shown in Figure 2.

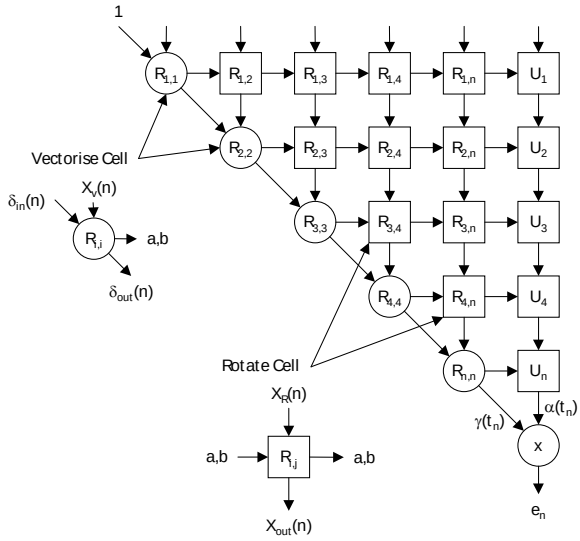

Figure 2: QR decomposition processing

To implement each vectorise and rotate cell separately would require a large amount of FPGA resources. However, the number of cells required can be reduced to give a linear configuration with a single vectorise cell and a number of rotate cells. The number of rotate cells can then be configured based on the processing speed required and the FPGA resources available [5]. An estimate of the processing resources [2], required for two different floating-point word lengths, are shown in Figure 3. This shows that only a small number of rotate processors can be implemented before the FPGA resources are fully utilized.

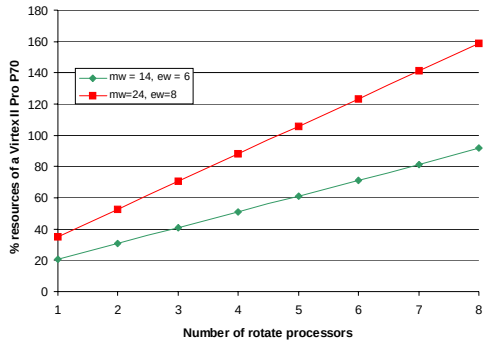

Figure 3: Resource requirements for QR core with varying number of rotate processors

The processing time to perform the QR decomposition is related to the number of array channels and the number of processing cells implemented. Figure 4, shows the processing time required for different numbers of array channels and numbers of rotate cells, for a FPGA clock speed of 125MHz and 64 input equations with data in IEEE single precision floating-point format (24 bit mantissa (mw) and 8 bit exponent (ew)).

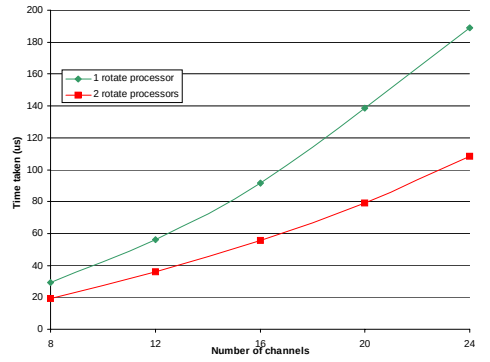

Figure 4: Time taken to perform QR Decomposition for varying number of channels

ABF system implementation in FPGA

The QR decomposition core is not the only component required within the processing system. A digital receiver and a beamformer, which consists of complex multipliers, is also required, along with a memory controller interface to external memory to implement a FIFO. Each of these components is required for each array element channel. These components are also all suitable for implementation in FPGA, giving a single processing technology solution

Hardware system realization

The processing solution requires ADC digitization hardware combined with FPGA processing hardware to implement the digital receiver systems. An ideal processing card for this is QinetiQ's Quixilica Venus VXS payload card, which provides five ADC channels, a large FPGA and external QDR and DDR memory.

The QR decomposition core is best separated from the digital receiver, to maximize the FPGA resources available, and hence to minimize the processing time required to calculate the adapted beam weights. An ideal system for the implementation of the QR is QinetiQ's Quixilica Callisto VXS switch card, which provides five Virtex-II Pro P50 FPGAs. This enables multiple beams to be calculated using multiple QR cores, each in a separate FPGA, or a larger number of rotate processors to be spread over multiple FPGAs, reducing the processing time required. Both of the processing cards provide connection of the FPGAs high-speed serial I/O to a VXS backplane, which enables rapid transfer of data between the FPGA processors.

Alternative applications

Most adaptive beamforming systems are currently targeted at radar systems. However, as the cost of the processing hardware and antennas is reduced they will become more applicable to communications systems and particularly mobile phone base stations. The techniques and hardware described are also applicable to SONAR applications and adaptive digital filtering.

Conclusions

Real-time adaptive beamforming is now possible in compact processing hardware. The QR decomposition technique for adaptive weight calculation is particularly suited to implementation in FPGA and FPGA cores are now available that reduce the system development time. These cores can be used with other DSP and floating point cores to provide a complete array sensor processing system in FPGA technology.

References

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