Future Prospects for Moore's Law

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Abstract:

"Moore's law" was the first widely-recognized indicator of progress in integrated circuit technology. It fits into a broader set of metrics that are used to characterize the detailed state of semiconductor technology today and is often used loosely as a surrogate for most of them. Some of these are the logic-gate/memory-bit-level metrics of cost, operating speed, active power, and standby power. For more than four decades, all of these have been improved at exponential pace principally by scaling the feature sizes of the device structures within ICs. Today, we label successive ~0.7x overall scaling milestones as semiconductor "technology nodes." The semiconductor industry's official definition, progress tracking, and future projections for IC technology nodes are documented in the International Technology Roadmap for Semiconductors (ITRS), which is updated annually. The updates are based on a consensus-building process conducted by Technology Working Groups with approximately 1000 international participants from industry (chipmakers and their suppliers), academia, and government. The principal purpose of the ITRS is to highlight future research and development needs in support of continued IC progress. It accomplishes this primarily by creating a (rolling 15-year-horizon) strawman extrapolation of recent trends for hundreds of IC technology parameters and color-coding them in terms of estimated risk of solution based on the best-guess level of R&D effort. Examples of the technology parameter projections, risk assessments, potential solutions, and other highlights of the 2003 ITRS are presented.

Of course, the scaling-based IC technology trends, such as Moore's Law, will eventually slow from their average pace of the 40+ years. However, we are still not close enough to any obvious "ultimate limits" to predict when there will be large departures from historic rates of progress in most of the high-level metrics. In 2004, even our "hp 90-nm CMOS" technology is still fairly far from "hard" physics limits, and significant "post-CMOS" research is underway. It is also important to note that the practical limits are not "sharp cliffs" and almost always involve cost and other product-level tradeoffs. In other words, it is not likely that progress will halt just because there are no viable purely technical solutions to further scaling, but because these solutions would cost more than a particular market will support. In this regard, it is quite likely that the development and/or one-time-engineering costs will be more prohibitive than incremental manufacturing cost. This is already becoming the case for many potential low-volume products. Another complication in forecasting even ultimate CMOS, much less a potential successor, is that the significant parameters characterizing the technology don't tend to saturate simultaneously. At a particular technology node, CMOS processes are developed in several flavors, optimizing the tradeoffs between various customer care-abouts such as speed, power dissipation, on-chip integration of diverse functions, and cost. Among all of the historical IC technology trends, the most obvious saturation to date has been in chip size. For example,

DRAMs used to quadruple bit count every three years based on nearly equal contributions from die area increase and device/area decrease. Now they are quadrupling the bits every four years with essentially no increase in die size. Thus, for DRAMs and most other ICs, growth in chip size is no longer supporting Moore's Law. However, if you were to regard thin-film-transistor flat-panel displays as "chips," you would conclude that chip area is still increasing!

Today, almost everyone agrees that we have hopeful potential solutions for practically extending general CMOS scaling to at least the "hp 32-nm node." At this node, minimum transistor gate lengths are projected to be in the 13-15 nm range, which is still within theoretical CMOS device limits. What makes people more nervous in this regime are things like affordable lithography, manufacturing control of device parameters, and interconnect resistivity. Of course, there is considerable debate about how much farther ultimate CMOS lies beyond that point and what, if anything, might take its place. Thus, each of the last few editions of the ITRS have put increased emphasis on highlighting the need for additional post-CMOS research. The Semiconductor Industry Association (SIA) is the U.S. sponsor of the ITRS and uses it as input for creating recommendations on technology strategy. Based on the 2003 ITRS and a recent ITRS gap analysis by the Semiconductor Research Corporation, the SIA has recently presented a recommendation to the President's Council of Advisors on Science and Technology for increased long-range research in nanoelectronics. In summary, the SIA believes that the IC industry faces two grand challenges worthy of very significant new federal funding: (1) scaling limits of "evolutionary lithography/thin-film manufacturing" and (2) scaling limits of "charge-transport devices/interconnect." Furthermore, the SIA suggests that these might be overcome through new and synergistic research in the under-funded broad areas of:

(1) "directed self-assembly" of complex structures with "nanoelectronics-functionality" (computation, communication, etc.) and
(2) "beyond (classical) charge transport" signal-processing/computational technology (e.g., based on quantum-states), respectively. The prospect is not necessarily for an abrupt disruption of incumbent CMOS technology, which will probably persist for a long time. A more likely scenario is the development of new technologies that will begin to complement CMOS in "hybridized nano-electronics" prior to any eventual full replacement of CMOS functionality.