Future Prospects for Moore's Law

Eighth Annual High Performance Embedded Computing Workshop

Lincoln Laboratory

September 28, 2004

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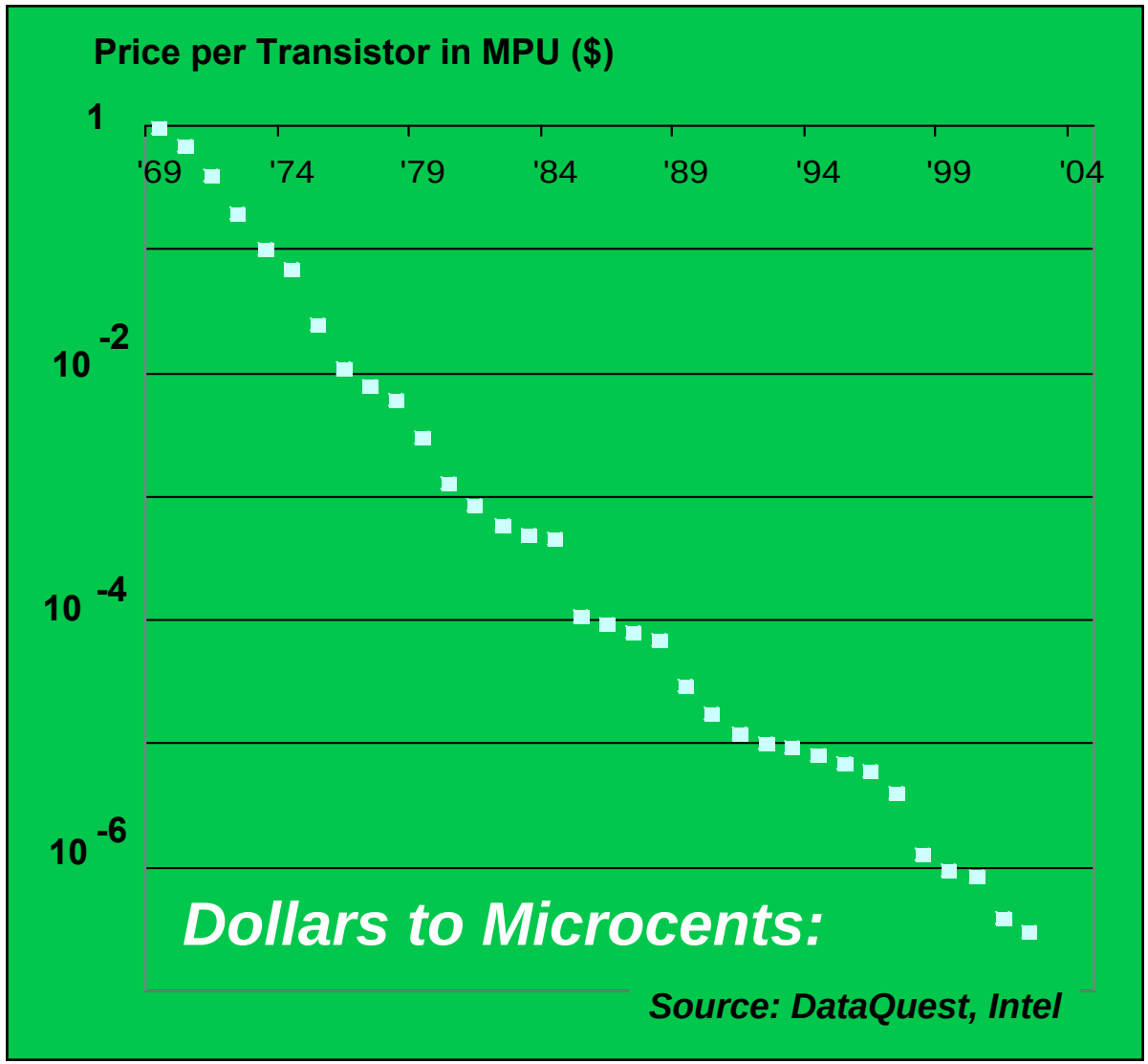
Generalizations of Moore's Law

Exponential trends in:

- More functions* per chip
- Increased performance
- Reduced energy per operation
- Decreased cost per function (*the principal driver*)

* *transistors, bits, etc.*



High-Level CMOS Technology Metrics – What are the Limits ?

- **Component Diversity** (integrated logic, memory, analog, RF, …)
- **Cost/Component** (e.g., μ¢/gate or μ¢/bit in an IC)
- **Component Density** (e.g., gates/cm^2 or bits/cm^2)
- **Logic Gate Delay** (time for a gate to switch logic states)
- **Energy Efficiency** (energy/switch and energy/time)
- **Mfg. Cycle Time** (determines time-to-market for new designs as well as rate of yield learning)

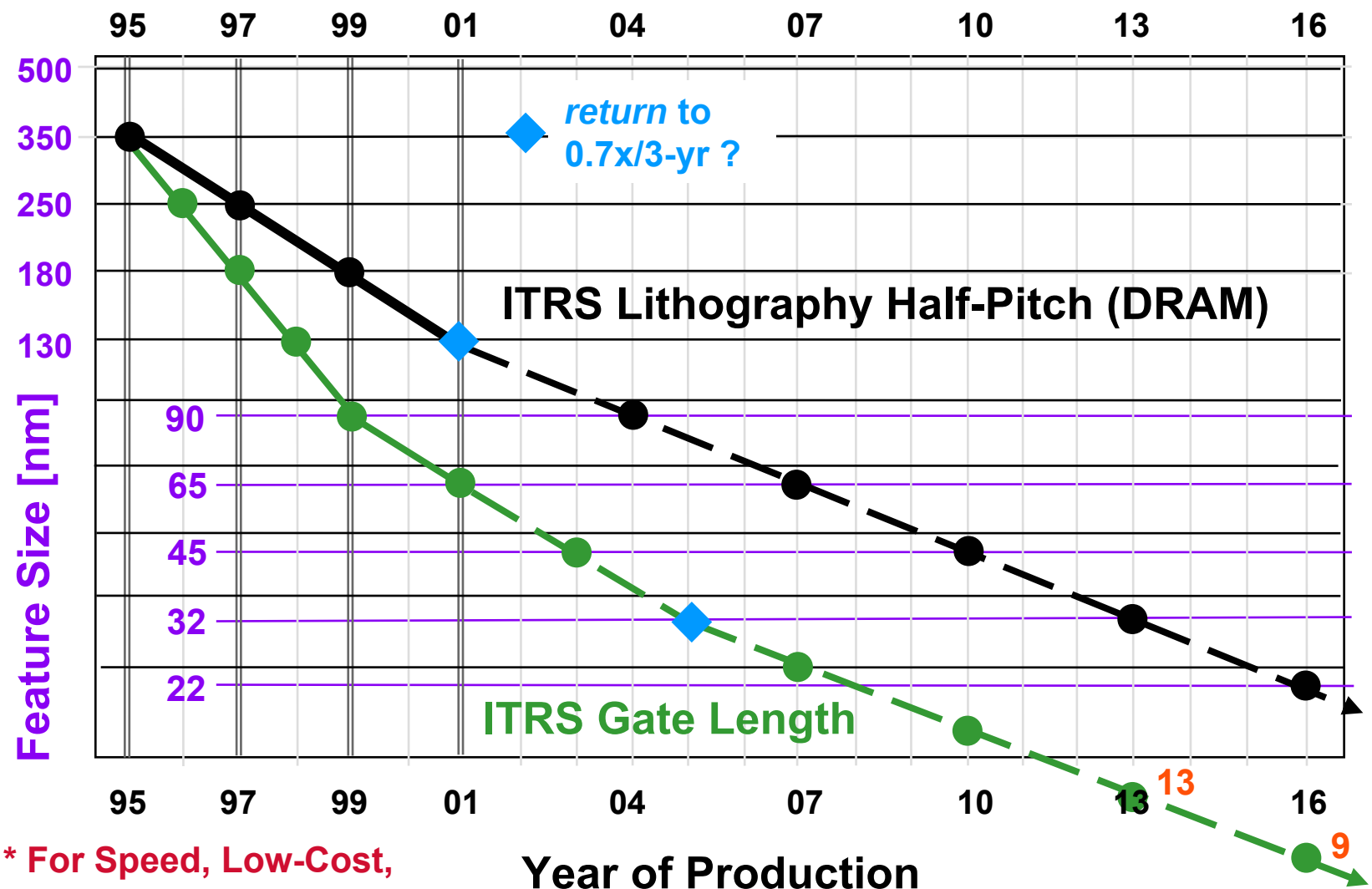
All of these are limited by multiple factors inter-linked into a complex "tradeoff space." We can only touch on a few of the issues today !

State-of-the-Art CMOS in 2004

- **ITRS Technology Node:** **90 nm** (half-pitch of DRAM metal lines)
- **4T-Gates/cm^2:** **37x10^6** (150 million transistors/cm^2)
- **6T-eSRAM bits/cm^2:** **10^8** (600 million transistors/cm^2)
- **Cost/Gate (4T):** **40 µ¢** (high volume; chip area = 1 cm^2)
- **Cost/eSRAM bit:** **10 µ¢** (high volume; chip area = 1 cm^2)
- **Gate Delay** **24 ps** * (for 2-input, F.O. = 3 NAND)
- **Switching Energy** **0.5 fJ** * (for inverter, half-cycle)
- **Passive Power** **6 nW** * (per minimum-size transistor)
- ***Min.* Mfg. Cycle Time** **10 days** (or 3 mask levels/day)

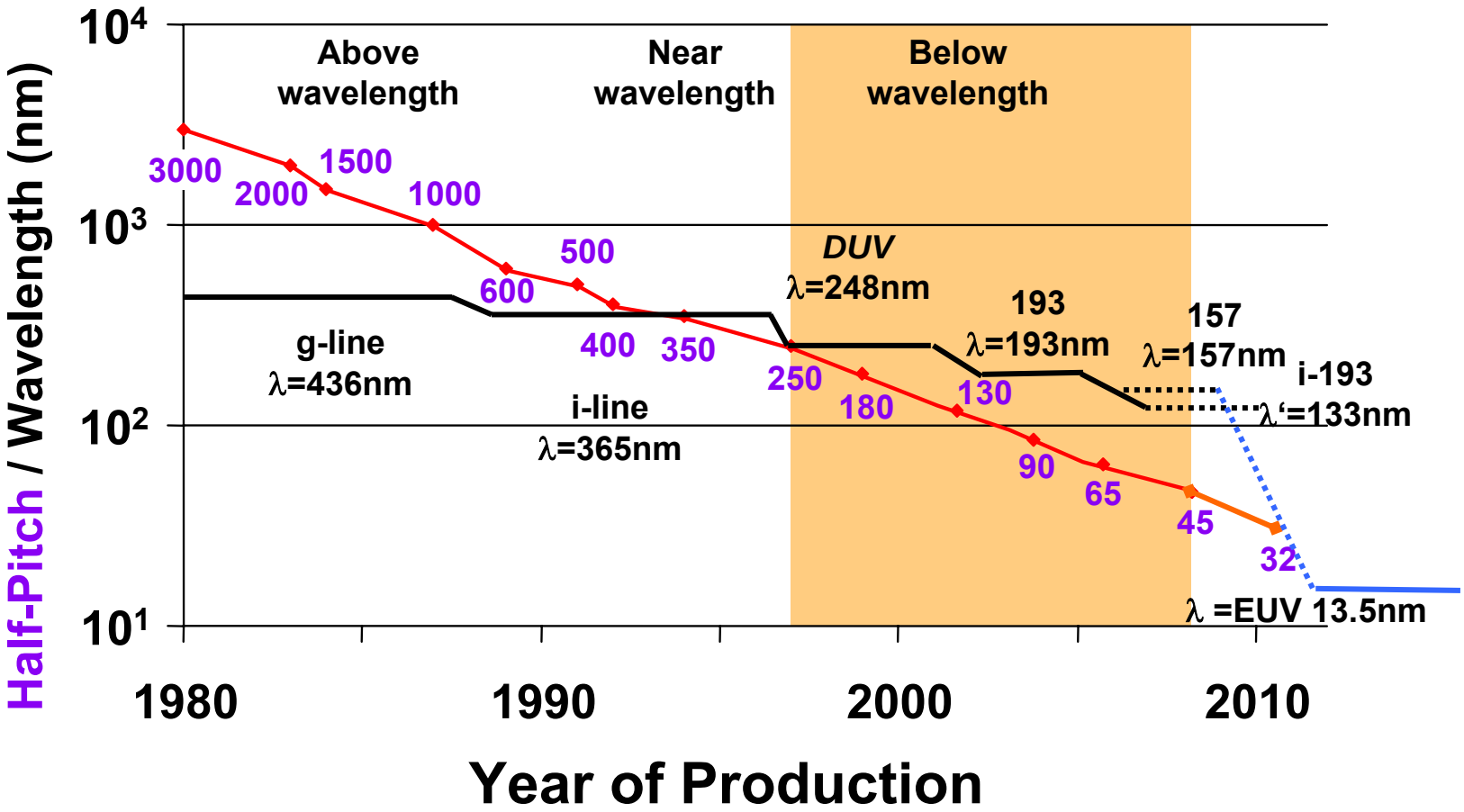
*** Values at extreme tradeoff for MPU application**

Scaling -- Traditional Enabler of Moore's Law*



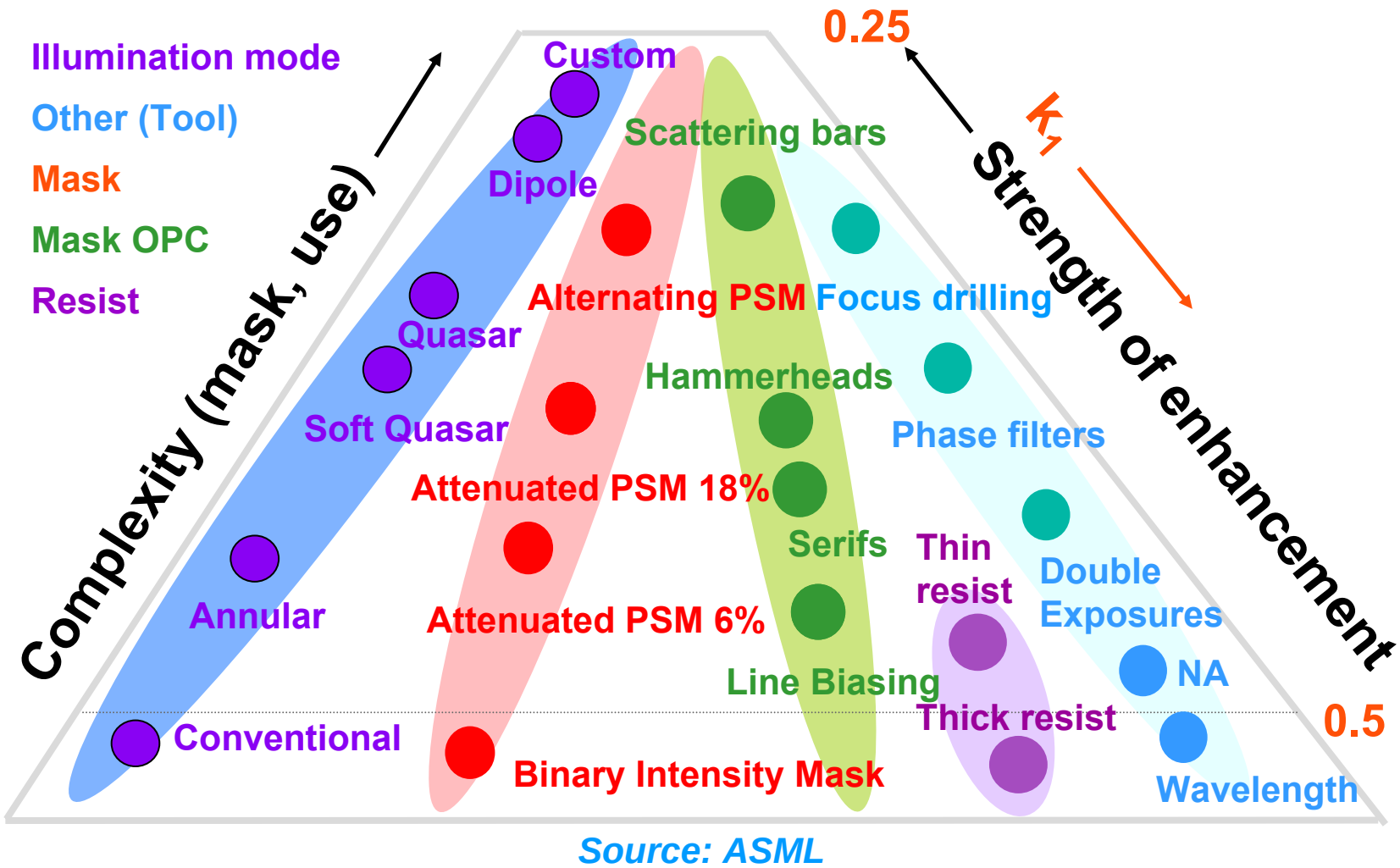
* For Speed, Low-Cost, Low-Power, etc.

Can We Extend the Recent 0.7x/2-year Litho Scaling Trend ?



For lithography, it's a question of cost and control/parametric-yield !

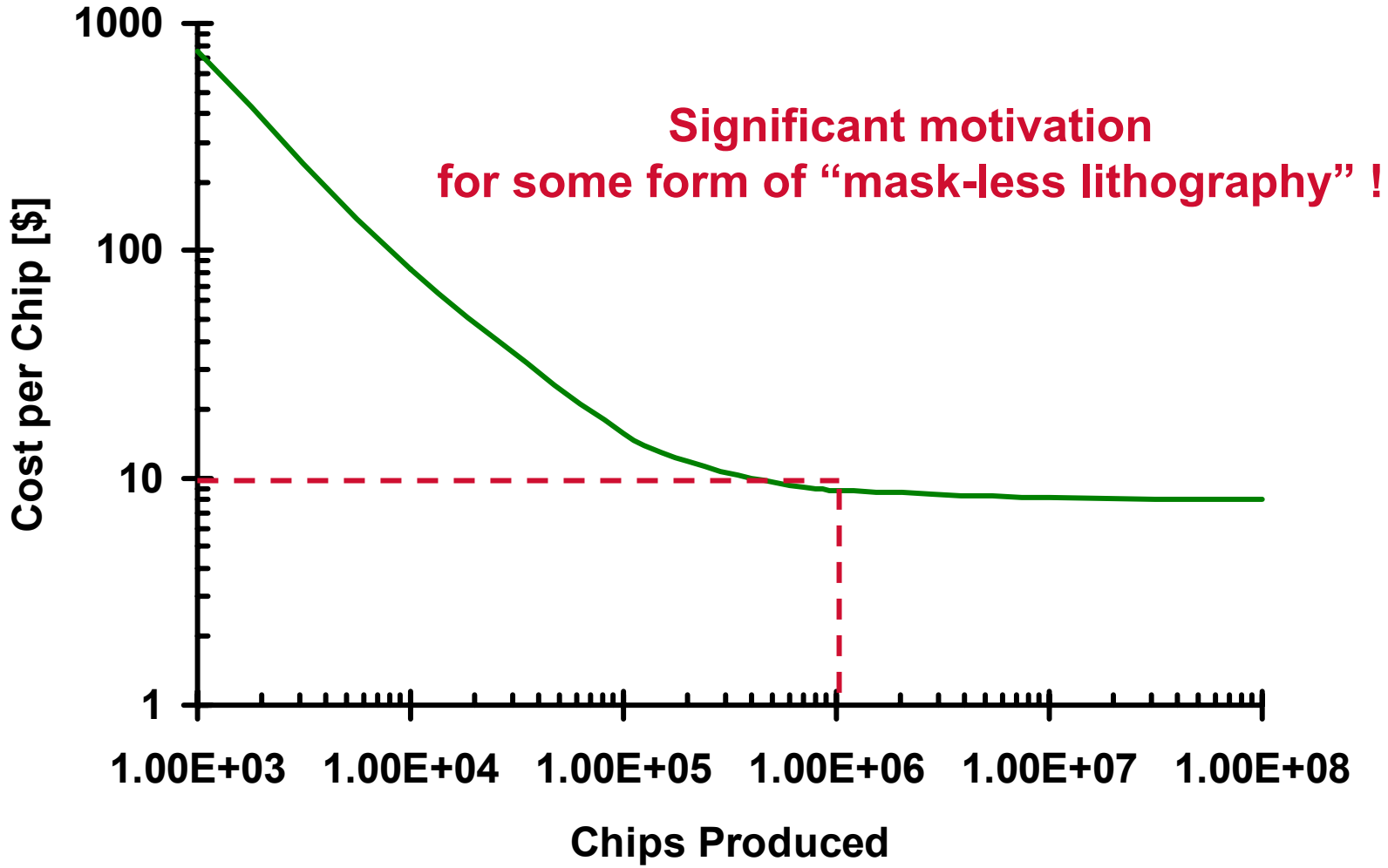
A "Bag of Tricks" for Optical-Extension



Source: ASML

Of course : increasing complexity → increasing cost !

Amortization of Mask Cost @ 130nm



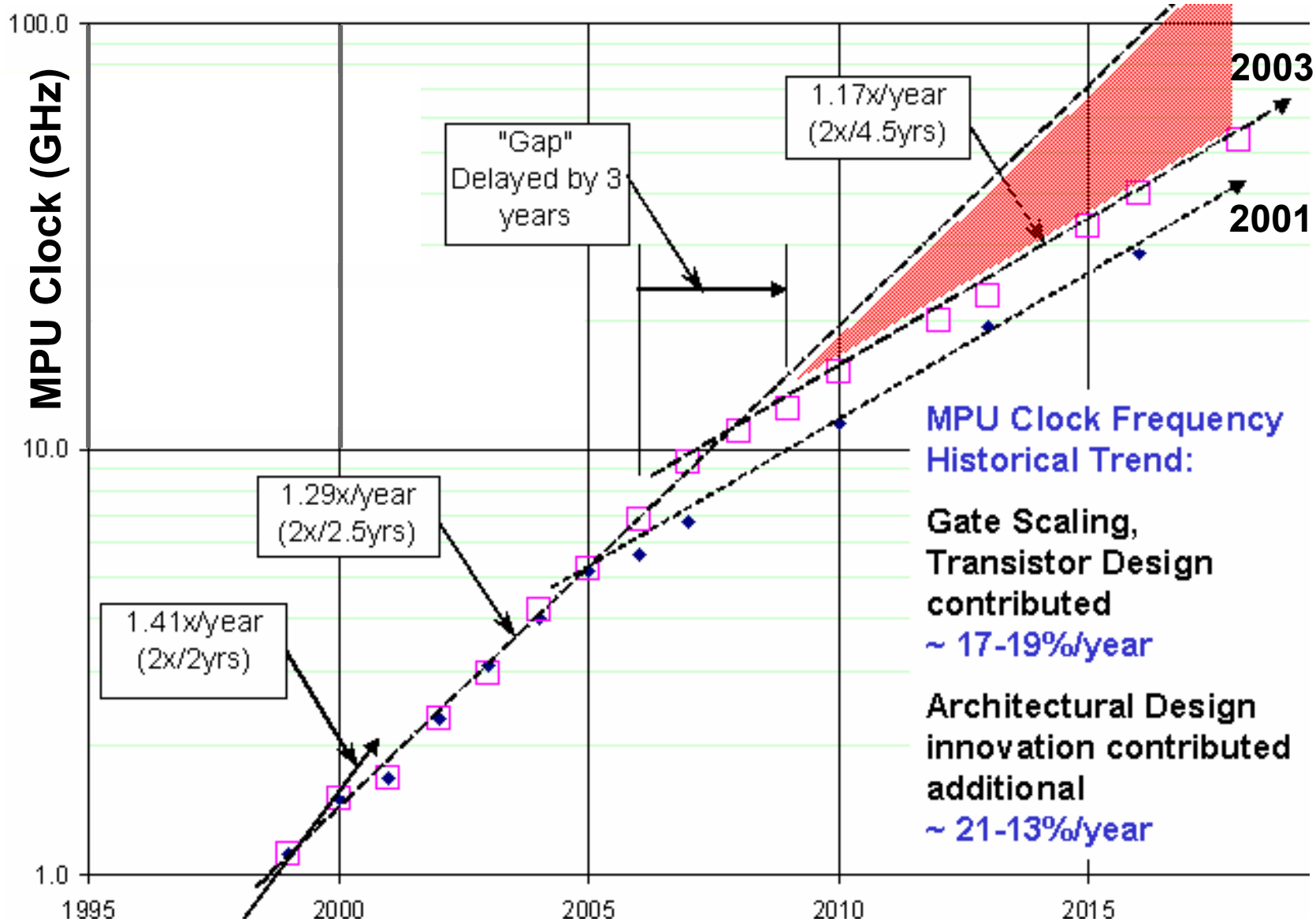
Significant motivation for some form of "mask-less lithography" !

~ 1 million units required to get within 10% of asymptotic cost !
(and getting worse with continued scaling)

Of course, overall scaling is limited by more than just lithography !

- Growing Significance of Non-Ideal Device-Scaling Effects:
  - I_{ON} vs. I_{OFF} tradeoff
  - unfavorable ρ and L scaling for interconnects
- Approaching Limits of Materials Properties
  - Heat removal and temperature tolerance
  - C_{MAX} vs. leakage tradeoff for gate dielectric
  - C_{MIN} vs. mechanical-integrity tradeoff for inter-metal dielectric
- Increases in Manufacturing Complexity/Control Requirements
  - cost and yield of increasingly complex process flows
  - metrology and control of L_{GATE}, T_{OX}, doping, etc.
- Affordability of R&D Costs
  - development of more complex and “near cliff” technologies
  - design of more complex circuits with “less ideal” elements

ITRS Tries to Address Top-Down Goals

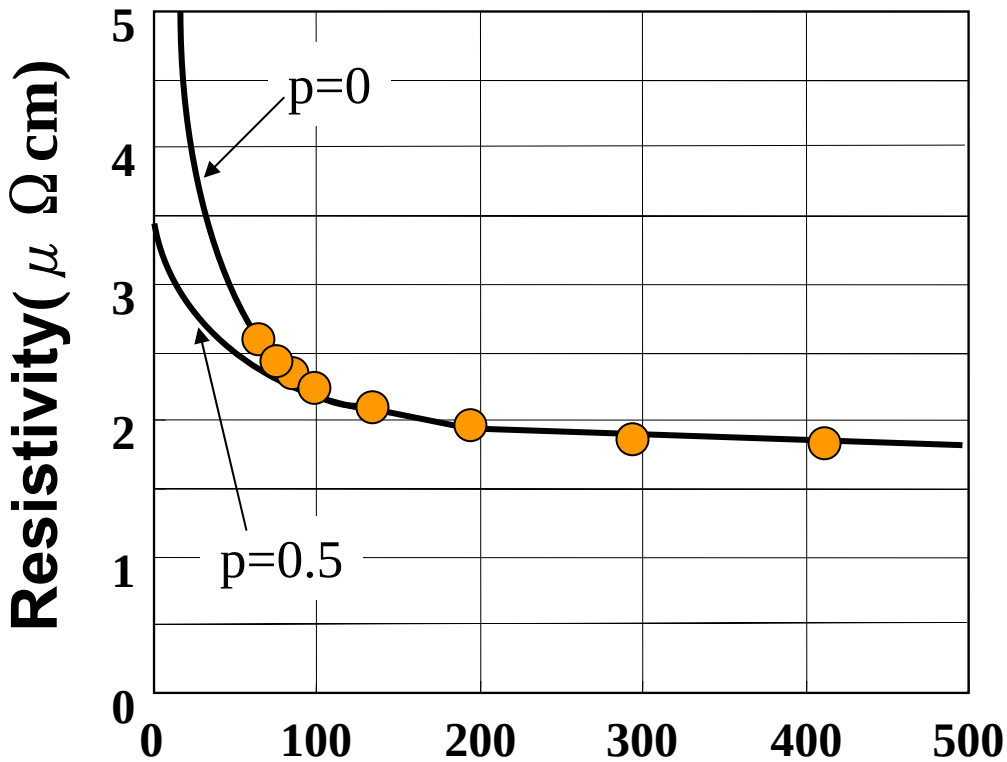


ITRS Highlights Scaling Barriers, e.g.:

Production Year:	2001	2004	2007	2010	2013	2016
Litho Half-Pitch [nm]:	130	90	65	45	32	22
Overlay Control [nm]:	45	32	23	18	13	9
Gate Length [nm]:	65	37	25	18	13	9
CD Control [nm]:	6.3	3.3*	2.2	1.6	1.2	0.8
T_{OX} (equivalent) [nm]:	1.3-1.6	1.2	0.9	0.7	0.6	0.5
I_{GATE} (L_{MIN}) [µA/µm]:	-	0.17	0.23	0.33	1	1.67
I_{ON} (NMOS) [µA/µm]:	900	1110	1510	1900	2050	2400
I_{OFF} (NMOS) [µA/µm]:	0.01	0.05	0.07	0.1	0.3	0.5
Interconnect K_{EFF}:	-	3.1-3.6	2.7-3.0	2.3-2.6	2.0-2.4	<2.0

Another Interconnect-Scaling Issue

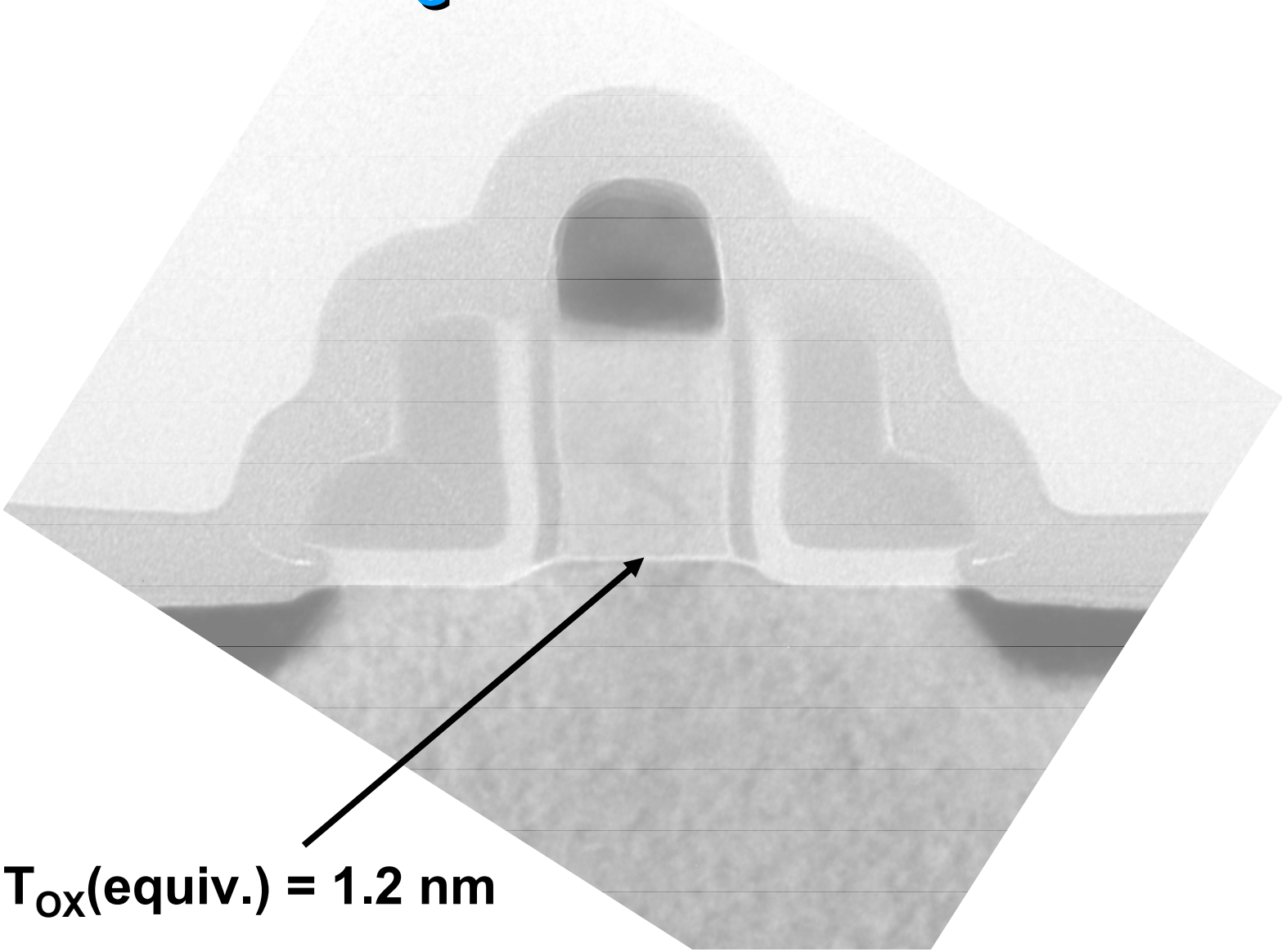
Wire width < mean-free-path of electrons



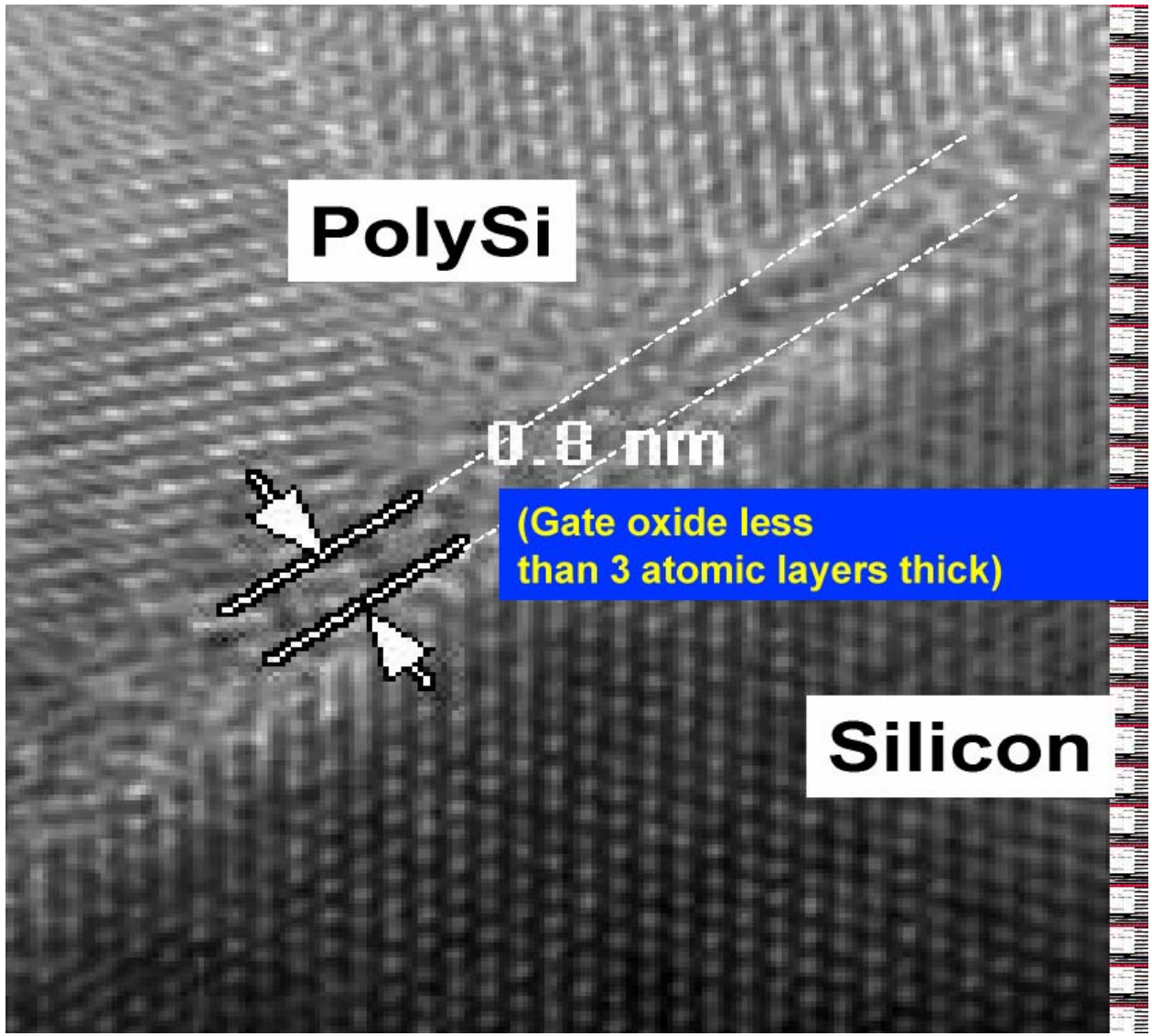
Surface scattering becomes dominant

p=0 (diffuse scattering)
p=1 (specular scattering)

2004 L_G = 37-nm Transistor



Can Some Hi-K Dielectric Replace SiON ?

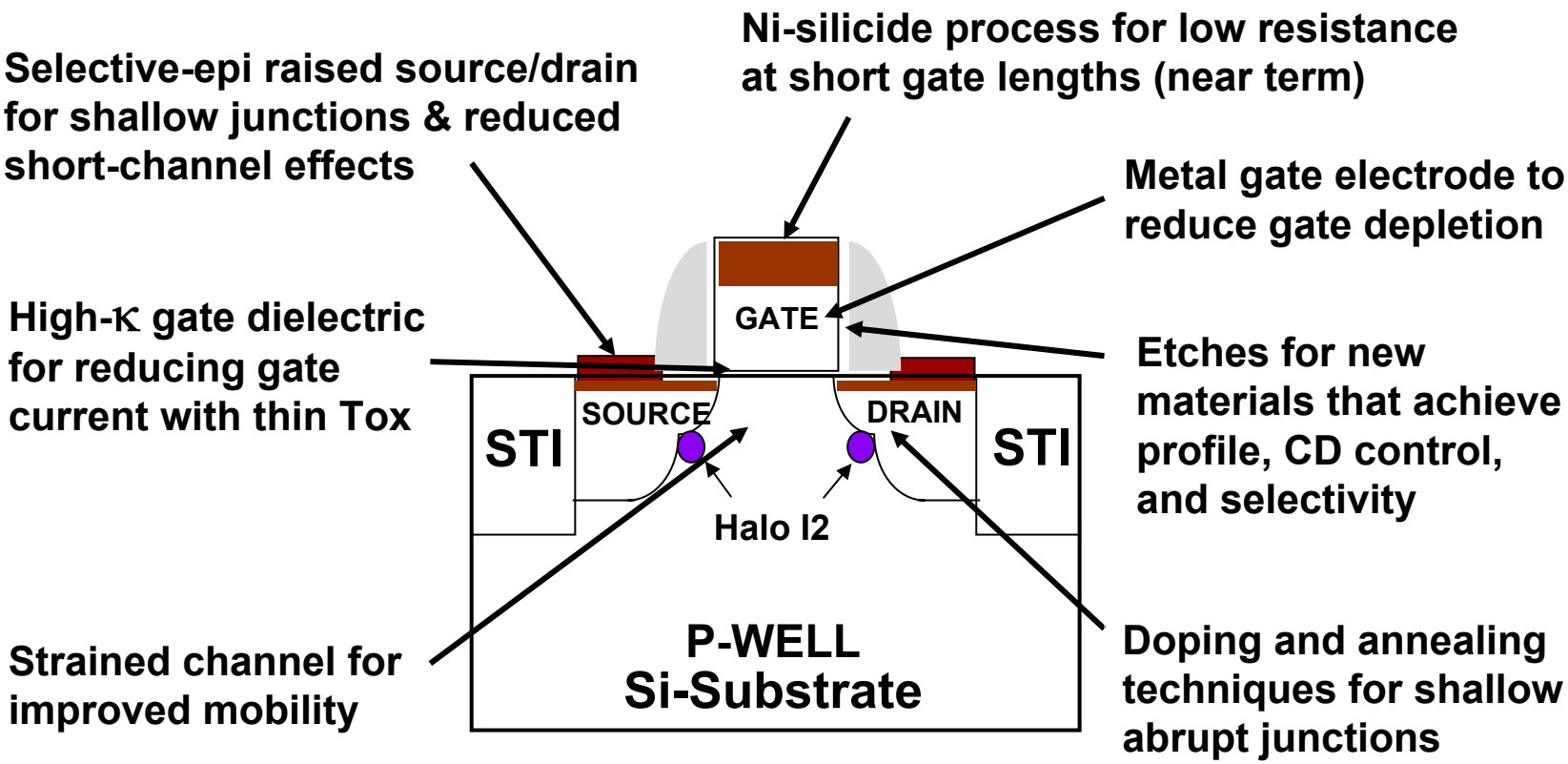


Sub-nm SiON:

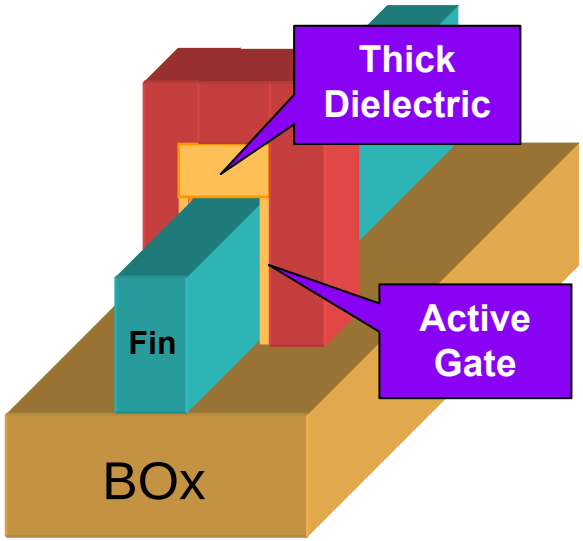
- mobility
- uniformity
- leakage

Source: Intel

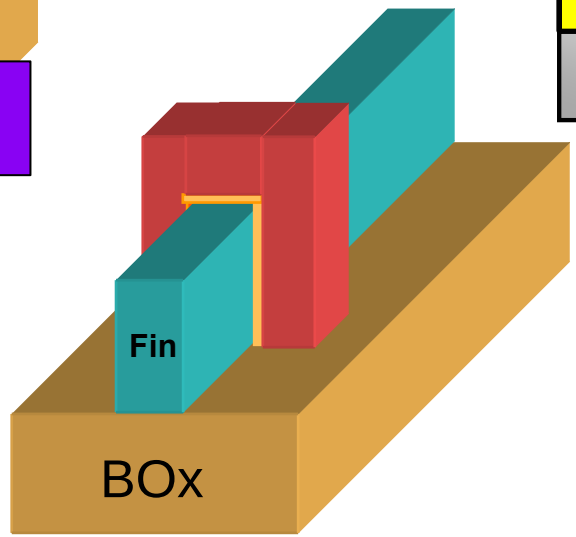
In general, continued transistor scaling requires new materials, processes, …



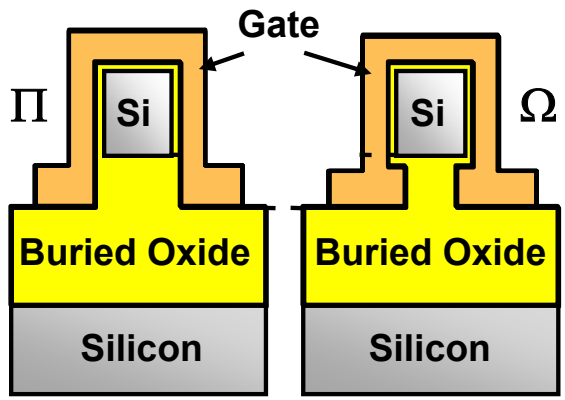
… and, eventually new structures

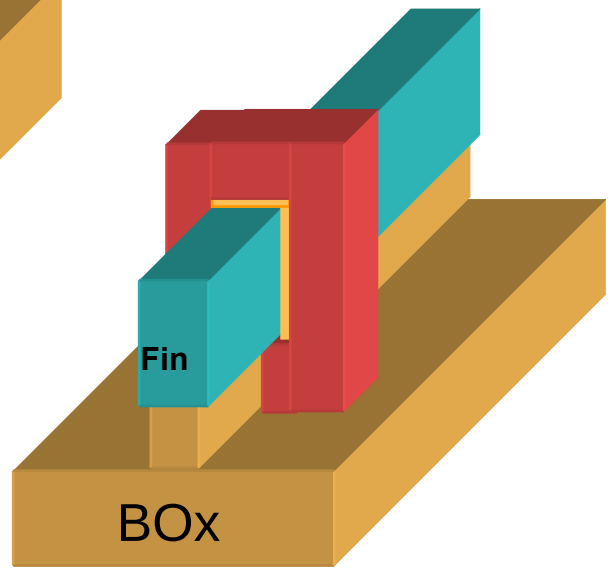


FinFET
2 Gates



Tri-Gate FET
3 Gates

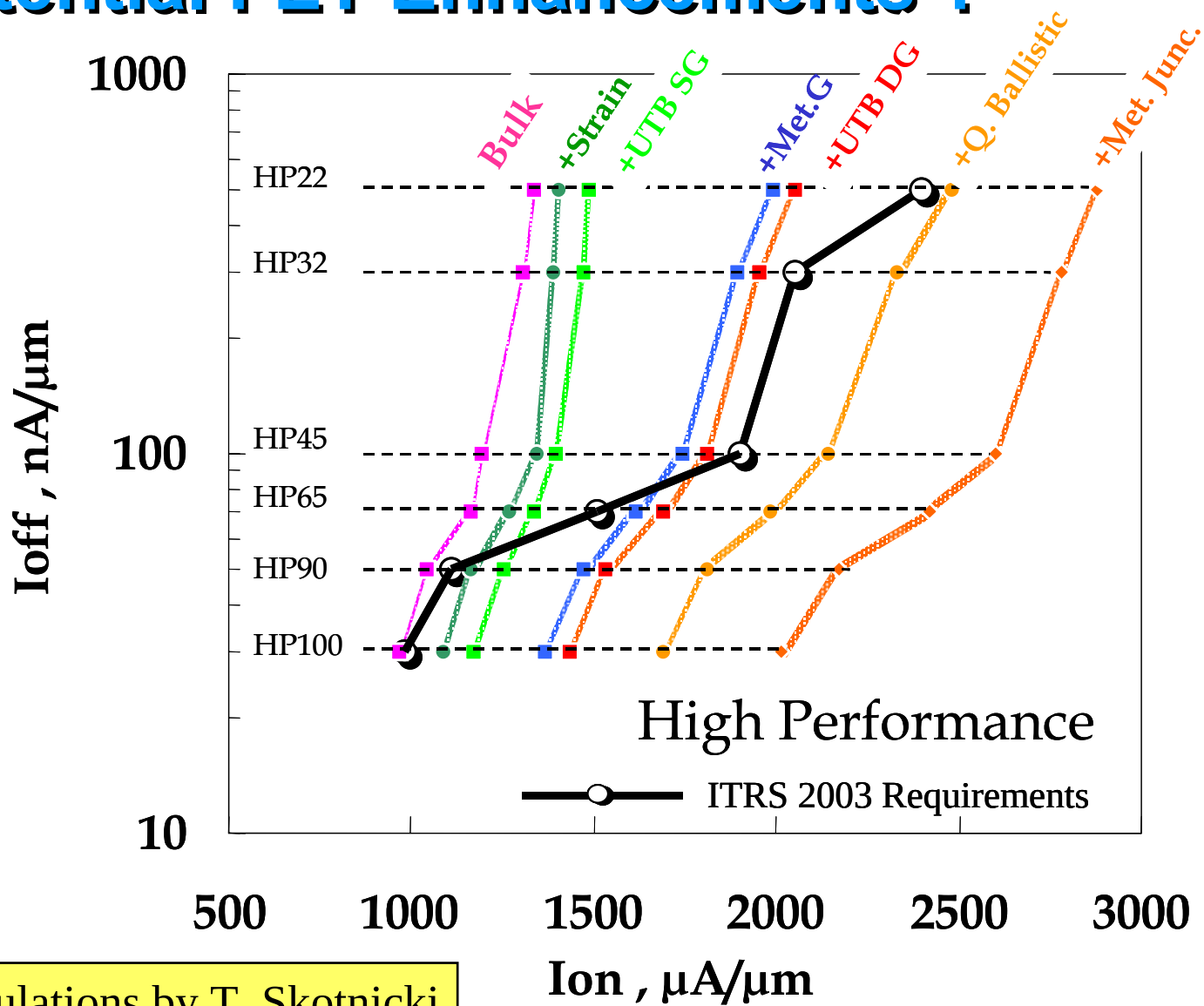




Π / Ω Gate FET
3+ Gates

Steps toward ideal "coax gate" →

Potential FET Enhancements ?



Calculations by T. Skotnicki

At PQE 2004, Professor Mark Lundstrom expressed the outlook:

"Sub-10nm MOSFETs will operate, but …

- on-currents will be ~0.5x$I_{ballistic}$, off-currents high,
- 2D electrostatics will be hard to control,
- parasitic resistance will degrade performance,
- device to device variations will be large,

and

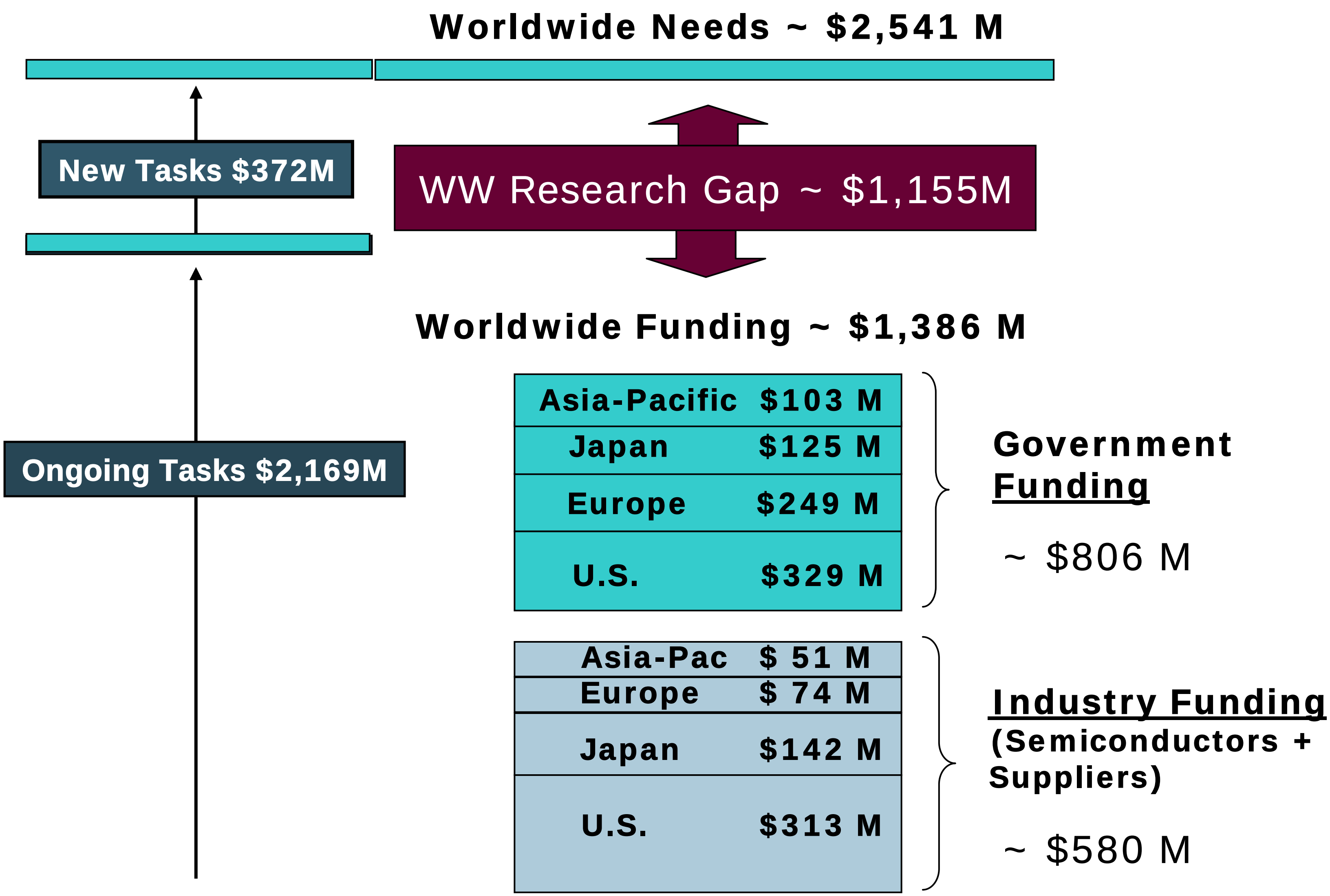
- ultra-thin bodies and hyper-abrupt junctions will be essential"

ITRS Assessment of Some Current Ideas for Successors to CMOS Transistors

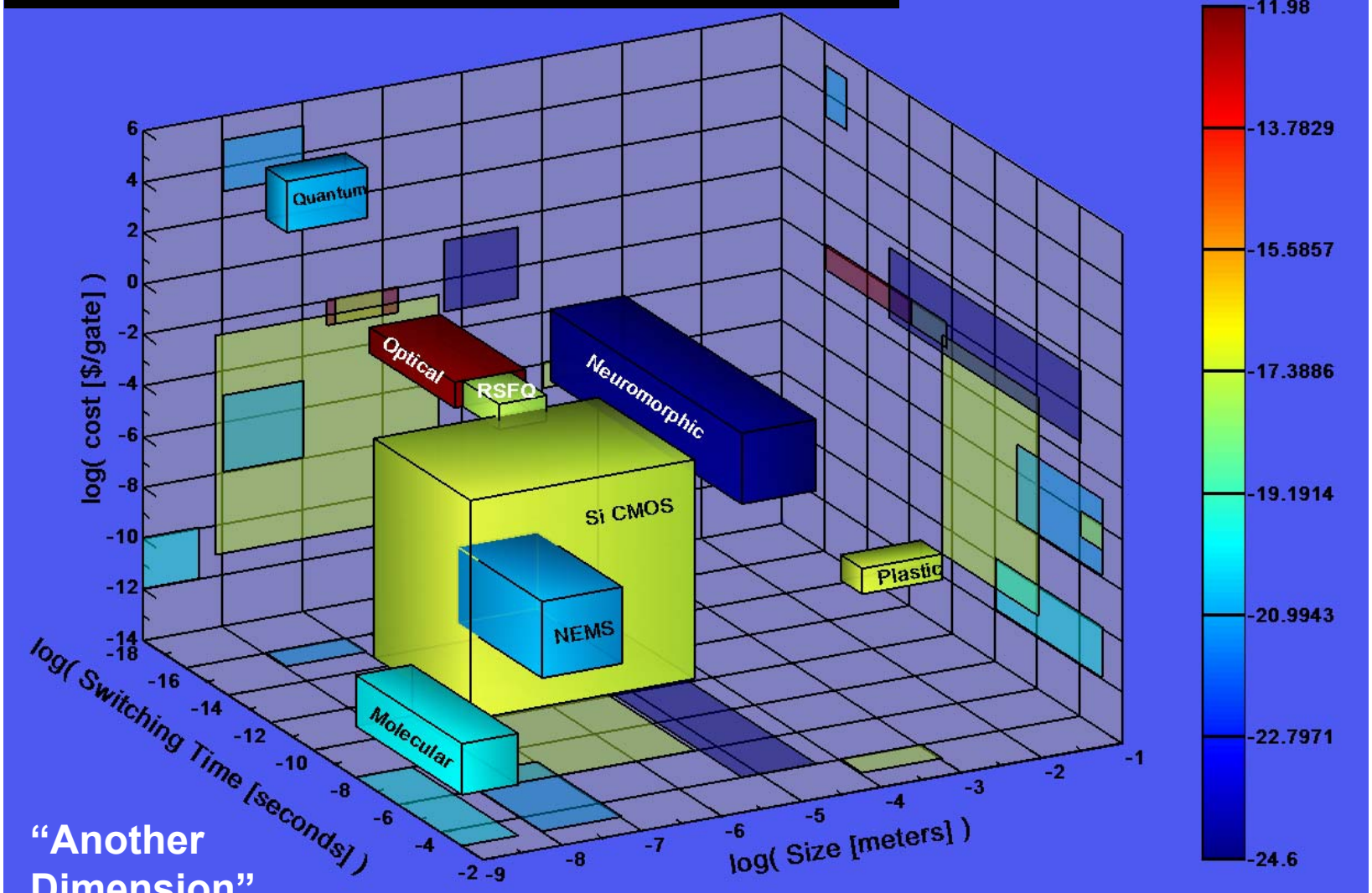
Logic Device Technologies	*Performance*	*Architecture compatible*	*Stability and reliability*	*CMOS compatible*	*Operate temp*	*Energy efficiency*	*Sensitivity Δ(parameter)*	*Scalability*
1D Structures	2.3/2.2	2.2/2.9	1.9/1.2	2.3/2.4	2.9/2.9	2.6/2.1	2.6/2.1	2.3/1.6
RSFQ Devices	2.7/3.0	1.9/2.7	2.2/2.8	1.6/2.2	1.1/2.7	1.6/2.3	1.9/2.8	1.0/2.1
Resonant Tunneling Devices	2.6/2.0	2.1/2.2	2.0/1.4	2.3/2.2	2.2/2.4	2.4/2.1	1.4/1.4	2.0/2.0
Molecular Devices	1.7/1.3	1.8/1.4	1.6/1.4	2.0/1.6	2.3/2.4	2.6/1.3	2.0/1.4	2.6/1.3
Spin Transistor	2.2/1.7	1.7/1.6	1.7/1.7	1.9/1.4	1.6/2.0	2.3/2.1	1.4/1.7	2.0/1.4
SETs	1.1/1.2	1.7/1.2	1.3/1.1	2.1/1.4	1.2/1.8	2.6/2.0	1.0/1.0	2.1/1.7
QCA Devices	1.4/1.3	1.2/1.1	1.7/1.8	1.4/1.6	1.2/1.4	2.4/1.7	1.6/1.1	2.0/1.4

No obvious candidates yet for a CMOS replacement !

SRC Research Gap Analysis (for <50nm)



ITRS Emerging Technologies ?

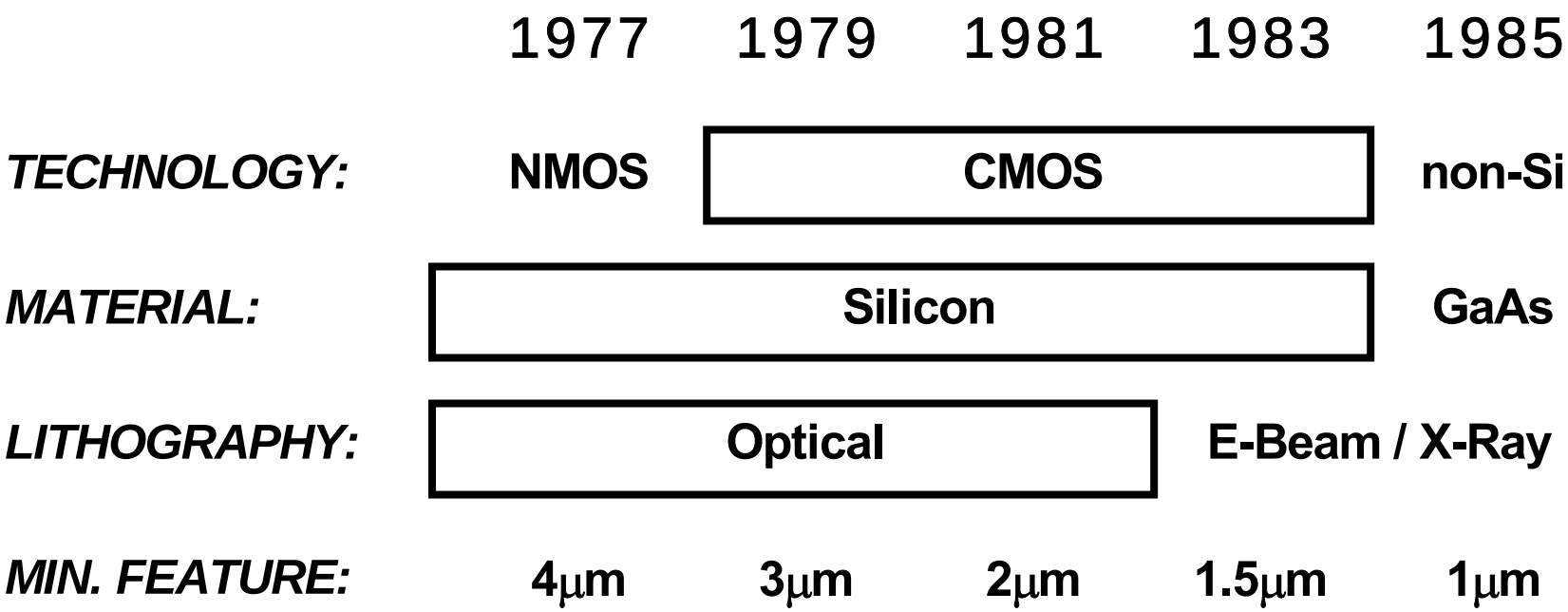


"Another Dimension"

→ Extending Moore's Law via Integrating New Functions onto CMOS

Why "Moore's Law" Is Still a Fun Topic !

A 1975 IC Technology Roadmap



What makes us think that we can forecast more than ~5 years of future IC technology any better today ?!!