Title of paper: "High Performance Embedded Computing using Field Programmable Gate Arrays"

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Submission: This paper is being submitted for open and closed sessions. Nallatech Inc wishes to present this paper as a poster presentation with a high performance embedded computing demonstration based upon Nallatech FPGA COTS products.

Area of work: Reconfigurable computing for embedded systems,
Algorithm mapping for high performance architectures,
Automated tools for embedded system development,
Case study examples of high performance embedded computing

Keywords: FPGA, COTS, Low Latency, Real Time, Scalability, Algorithm, Reconfigurable, Tools, Embedded Systems, High Performance, Architecture

Abstract

Ongoing commercial and technology needs are driving increasingly demanding performance requirements for new embedded processing systems. Over the course of the last two decades, embedded systems tasked with data, image and signal processing have utilised consecutive generations of conventional processing technologies such as RISC, DSP and CISC processors. The processing capabilities of these devices have increased steadily in accordance with Moore's law – providing scientists and engineers with the ability to process large amounts of sensed data and solve computationally intensive problems for a number of end-markets, including Aerospace and Defence, Communications Infrastructure and Imaging.

Advances in sensor technologies available now, and predicted over the next few years are providing engineers with the ability to implement sophisticated embedded processing systems featuring increased bandwidths, functionality and data rates. As the aggregate throughput requirements for embedded systems approaches GOPS, these types of processing technologies become unsuitable since performances can only be met by concatenating processing blocks in a pipeline architecture. This incremental approach to boosting system performance has limitations, and is often an unacceptable solution, particularly for applications constrained by factors such as size, weight, power and environmental conditions. These design considerations represent significant challenges to the system engineer, particularly when the application is intended to be used as part of an embedded system operating in real time, where system complexity can be compounded by environmental conditions such as temperature, altitude and vibration.

Assuming that these problems are overcome, or at least manageable, applications demanding real time operation cannot function with system latencies in the order of seconds. Compromises are possible through reductions in data rate and sensor resolution; however these sacrifices only contribute to overall system performance degradation. High performance custom solutions such as ASICs have become prohibitively expensive, with development times and costs far greater than competing technologies. There is, therefore, a requirement to develop and utilise new types of processing technologies such as Field Programmable Gate Arrays (FPGAs) which are able to alleviate many of the economic and technical challenges associated with high performance embedded processing systems.

Over the last decade, the performance capabilities of FPGAs have increased exponentially. Leading vendors such as Xilinx and Altera have improved the functionality of their reconfigurable devices through the inclusion of memory, processors, multi-gigabit transceivers, and multipliers to the basic FPGA architecture. The result is a flexible, high performance processing device able to perform low latency, parallel processing tasks with low power consumption.

In order to exploit the obvious benefits of FPGA technology in embedded systems, Nallatech has developed a range of FPGA-centric COTS products based upon the company's modular DIME-II™ architecture capable of TeraOPS performance. Customers using Nallatech products such as the BenNUEY-PC104+ shown in Figure 1, are able to harness the full capability of advanced Virtex-II and Virtex-II Pro Xilinx FPGAs.

With a range of motherboard form factors including PC104*plus*, VME, PCI and cPCI and a catalogue of plug and play DIME-II™ modules, embedded system developers can quickly build a flexible, high performance processing system tailored to the requirements of a specific application.

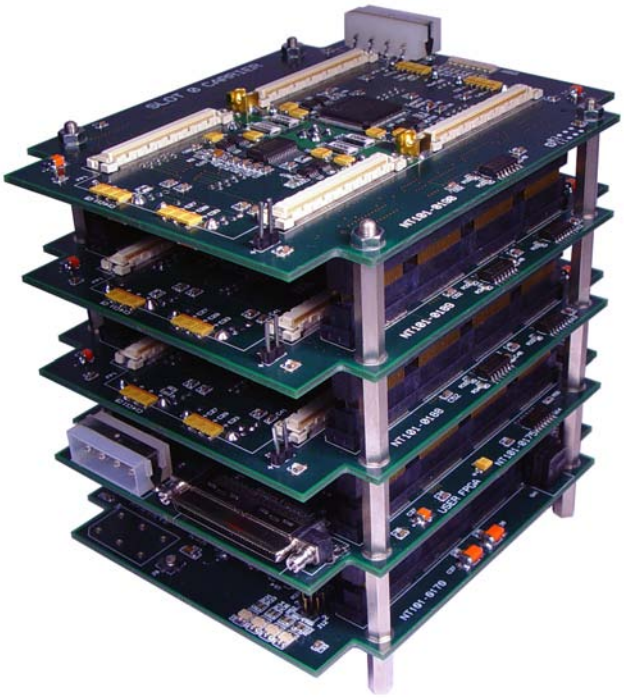

Figure 1 – Nallatech PC104*plus* COTS motherboard

To date, Nallatech products have been utilised in a range of embedded applications including Unmanned Aerial Vehicles (UAVs), Imaging, RADAR and satellite systems. Under normal circumstances, a number of conventional processors would have been used to deal with the fast data processing requirements of such systems; however FPGAs are now a cost effective alternative.

Figure 2 shown below is a screenshot of a Nallatech demonstration using a BenNUEY motherboard populated with three DIME-II modules featuring two 2V6000 Xilinx FPGAs – a total of seven 2v6000 FPGAs including the onboard BenNUEY FPGA. The demonstration implemented a simple fractal generation algorithm. It is an iterative process that determines when a function exceeds a given threshold. It was applied to a nominal 512 x 512 array, with the resulting data displayed on the host computer.

The original algorithm, a well understood mathematical calculation often used in benchmarking exercises such as this, was implemented in standard C code executing on an Intel Xeon 1.8 processor. The same algorithm was implemented on the Nallatech BenNUEY FPGA motherboard using Nallatech's own IEEE-754 floating point cores, with the data transfer between the host and the multiple devices handled Nallatech's FPGA network communications tool called "DIMEtalk".

Table 1 summarises the results that were achieved using firstly the Intel Xeon processor, and then the Nallatech FPGA system, which was attached to the host PC via the PCI bus.

Processor	GFlops	Power (Watts)	GFlop / Watt
Intel Xeon	0.17	40	0.004
FPGA System	24	20	1.2

Table 1 – Fractal Calculation Results

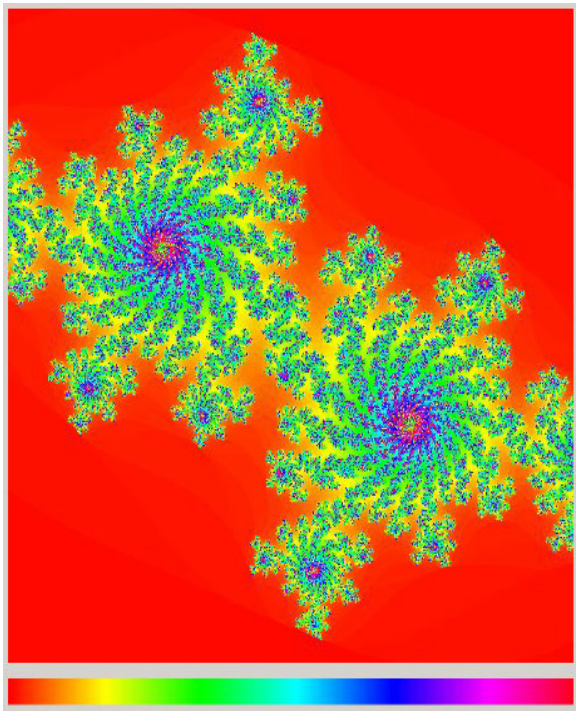

Figure 2 – Fractal Pattern

The results of this experiment clearly demonstrate that the FPGA based processing system is far superior in terms of computational performance and power consumption than the Intel Xeon processor. The use of reconfigurable resources, in this case to speed the inner iterative loop of the fractal calculation, resulted in a 240 times improvement in performance in the same physical volume. This means that, in theory, one 2U box could replace the processing power of twelve 6 foot high racks. Also, the power consumption per GFlop of computing performance was 300 times better.

Whilst this is a particular application, and hence cannot be assumed to be directly applicable to all examples, it does demonstrate the performance levels attainable using FPGAs. It is reasonable to assume that most similar internal algorithms could be scaled up in performance by one or two orders of magnitude.

The key advantages of FPGAs in these systems are increases in per-device performance and reduced per-device power consumption – i.e. improved performance density. However, the design of FPGA-based systems can be more demanding than the microprocessor-based solutions. COTS FPGA hardware solutions and high-level FPGA algorithm design tools, such as those provided by Nallatech, have improved this position, helping designers to reduce development times, cost and risk when developing high performance embedded systems.

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