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Title:	Processing Challenges in Shrinking HPEC Systems into Small UAVs
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The best-known unmanned aerial vehicles (UAVs), Predator and Global Hawk, are large, multi-million dollar aircraft managed as theater/national assets. With synthetic aperture radar (SAR), electro-optic/infrared (EO/IR), and signals intelligence (SIGINT) payloads, these UAVs have proven their worth in battlefields from Bosnia to Afghanistan and Iraq. This success has led to surge in proposed UAV missions and designs using a layered approach with multiple classes of UAVs to provide persistent narrow and wide ISR (intelligence, surveillance, reconnaissance) coverage. Programs such as the Future Combat System (FCS) include a large role for tactical UAVs, small UAVs, and unmanned ground vehicles (UGVs). The smaller, cheaper unmanned vehicles can be deployed at the brigade or company level to "see over the next hill." With many vehicles and many sensors, network bandwidth becomes an issue. So future UAVs will include aided/automatic target recognition (AiTR/ATR) capabilities to reduce both communication bandwidth and latency.

Large UAVs such as Global Hawk and Predator have been successful using today's HPEC solutions. Global Hawk currently uses a 9U VME system with PowerPC processors for SAR and EO/IR processing, while the Predator is a bit smaller, using a 6U VME system for TESAR processing. The challenge is to provide similar processing power for much smaller UAVs, many of which have less than ½ the payload weight and ¼ the volume of the Predator (see examples in Table 1). Note that only a small portion of the payload is allocated for signal and image processing. For example, the TESAR image processor on the Predator is just 55 pounds, less than 1/10 of the total payload weight.

Table 1: UAV Payloads

UAV	Global Hawk	Predator B	Heron A	Hunter	Eagle Eye	Fire-scout	Sentry	Dragon Warrior	Dragon Eye
Length (ft)	44.4	36	26	22	17	23	8.4	10	3
Wingspan (ft)	116	66	54	29	17	20	12.8	9	3.8
Height (ft)	14	9.5	5.9	5.6	5.5	9.5	4	5	1
Payload Weight (lbs)	1000	800	550	250	200	200	75	35	5
Max Altitude (ft)	65k	50k	25k	15k	20k	20k	15k	4k	1.2k
Sensors	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR	EO/IR	EO/IR
Endurance (hrs)	36	36	36	10	5	4	3	3	1
Max Airspeed (kts)	320	220	120	100	220	120	100	70	35

In the past, we have relied on Moore's Law to help us out. We could wait a couple of years and the technology improvements in the electronics would have enabled significant shrinking of size. However, we've come to a point where Moore's Law effects still increase absolute performance, but not performance per Watt, per pound, or per cubic foot. Although the number of transistors available is increasing, the power consumption is increasing at almost the same rate (see figure 1). The increased infrastructure to handle the power distribution and heat extraction incurs a penalty in size and weight. Alternative approaches are needed.

One approach is to leverage field-programmable gate arrays (FPGAs) as programmable processors. For some front-end signal and image processing functions, FPGAs have been shown to provide a 10-20 fold performance boost over a PowerPC G4 processor. However, some front-end tasks, like filter weight computation, and most back-end processing still performs much better on a PowerPC processor. Given the higher power consumption of an FPGA, there is a limit on the number of FPGAs that can be used in a system. In trying to fit the most processing power in the smallest space for a given application, the trick is not only trying to find the optimum balance between FPGAs and PowerPCs, but also exactly which model of each chip to choose.

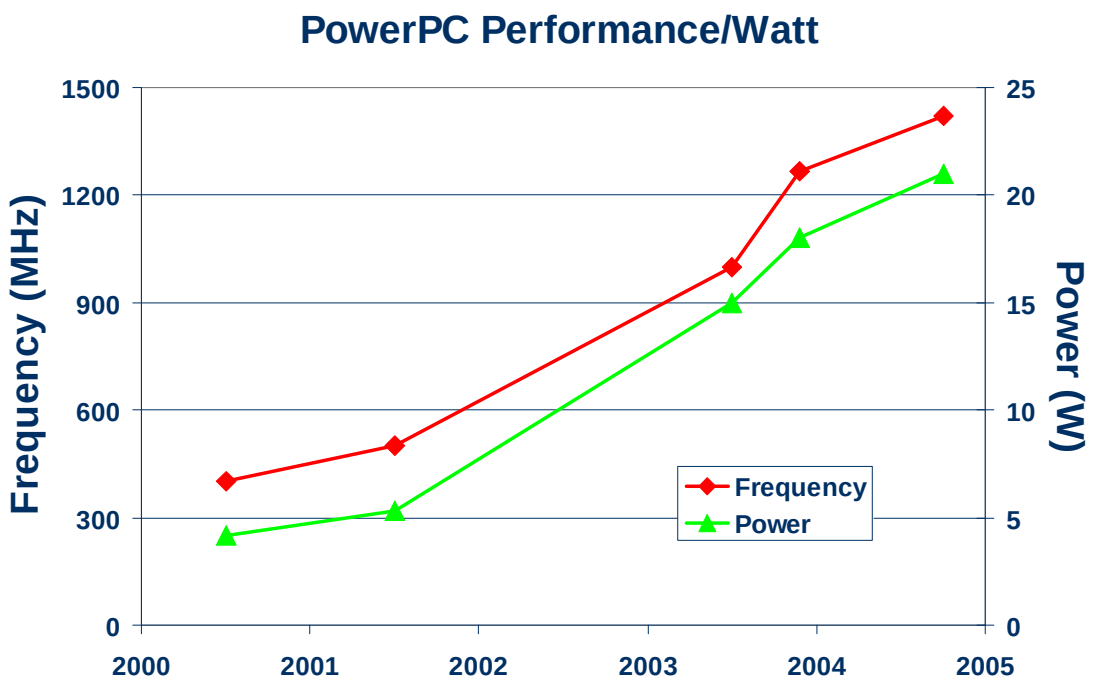

Figure 1: PowerPC frequency and power consumption.

Most evaluations of FPGA chips focus on the number of logic cells, slices, and processor blocks. An example comparison of Xilinx FPGAs is shown in Figure 2. For embedded signal and image processing applications, more critical elements tend to be the number of multiplier blocks and the size of the block RAM. This leads to different component selection, as shown in Figure 3.

The slot limitations on space-constrained systems also lend to integration of the analog-to-digital conversion and general I/O with the processing. This is especially important for multi-channel systems. That sensor I/O can be part of the base-board design along with processors or be a separate mezzanine card. A separate mezzanine card gains board real estate but restricts the power and cooling available to each card.

This presentation will provide a detailed set of trade-offs in computational capabilities, I/O capabilities, and memory capacities distributed between FPGAs and PowerPCs for sample applications of SAR image formation and SIGINT channelized receiver throughout.

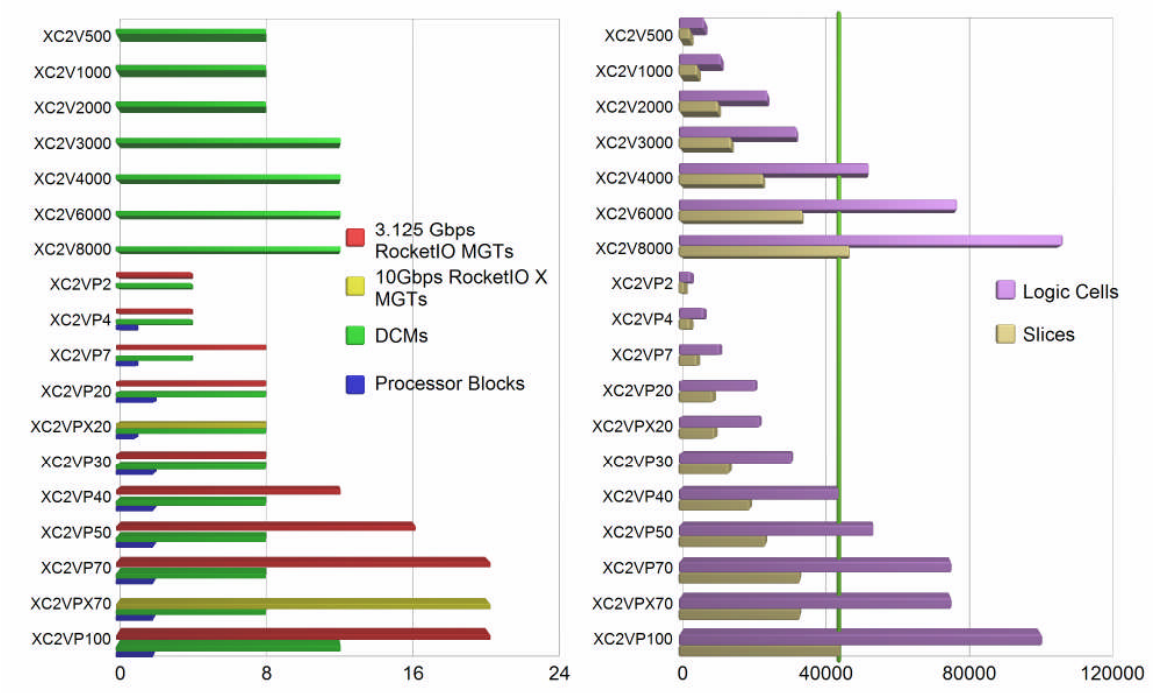

Figure 2: Typical comparison of FPGA attributes.

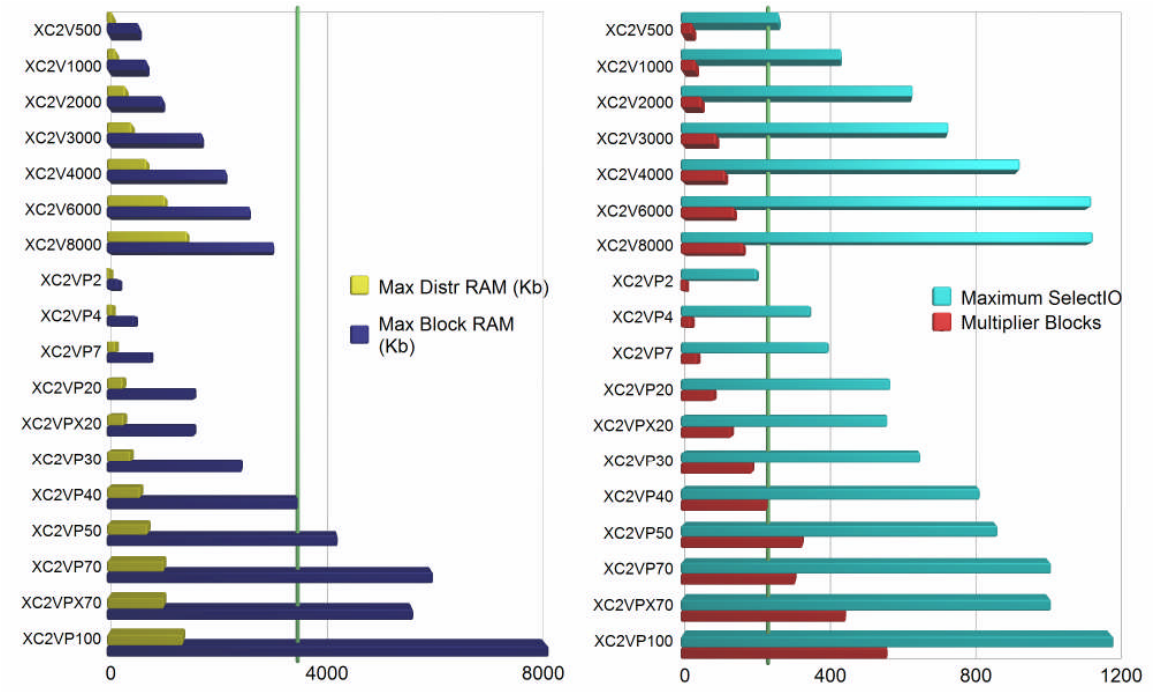

Figure 3: Focusing on RAM and multiplier blocks for FPGA computing.