Liquid Architecture

Microarchitecture Optimization for Embedded Systems

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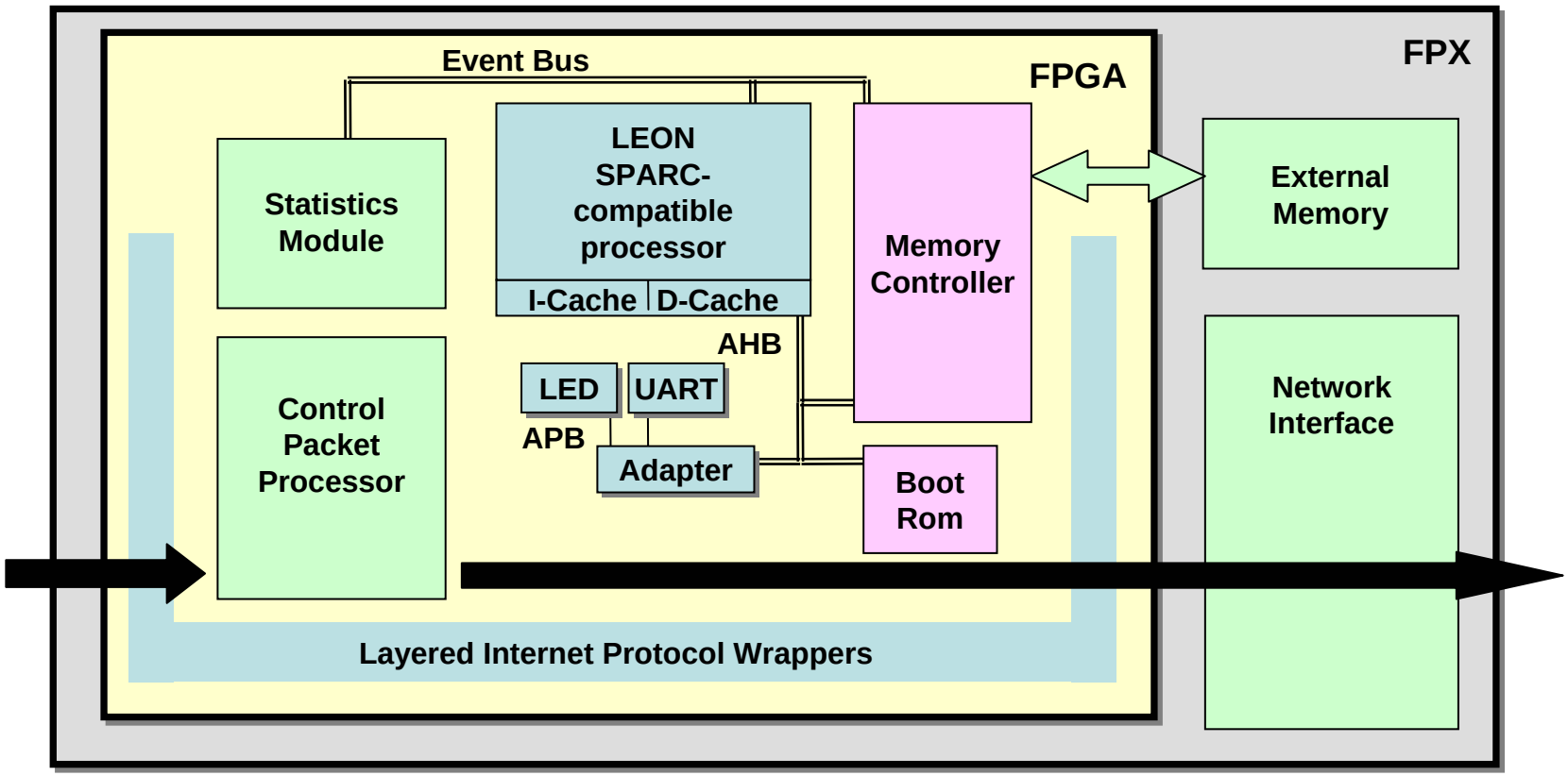
Liquid Architecture

- Configurable architecture that can adapt to needs of particular application
- E.g., within an FPGA
  - Soft-core processors
- E.g., as an embedded processor
  - Tensilica supports configuration at fab time
  - Stretch support configuration at run time
- Today's discussion is on performance analysis and configuration choice

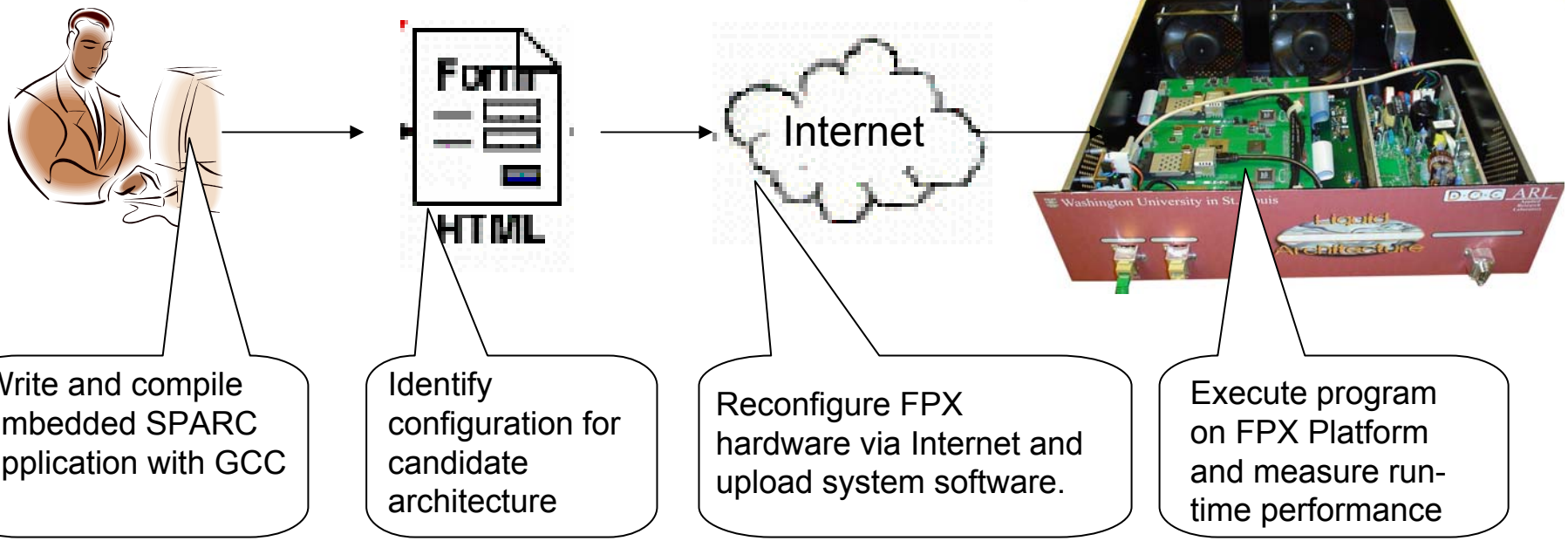
Block Diagram



Microarchitecture Configurability

- Instruction set
- Memory subsystem
  - Cache size (I and D)
  - Associativity
  - Cache line size
- Co-processor(s)
- Instruction pipeline
- Full HDL source is available

Design Flow

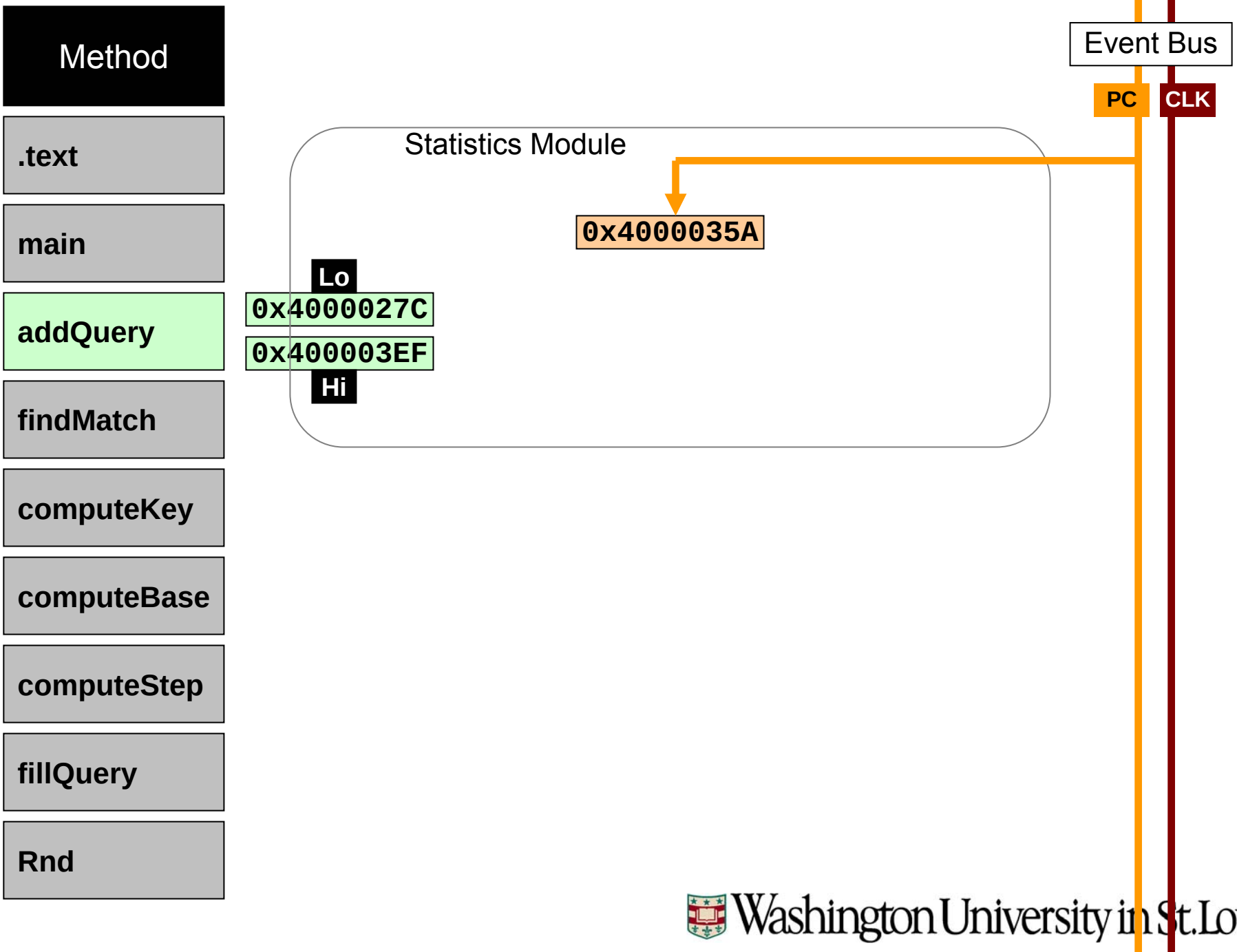

Internet
HTML
Write and compile embedded SPARC application with GCC
Identify configuration for candidate architecture
Reconfigure FPX hardware via Internet and upload system software.
Execute program on FPX Platform and measure run-time performance

Method	Time / Cycles
.text	☐
main	☐
addQuery	☑
findMatch	☐
computeKey	☐
computeBase	☐
computeStep	☑
fillQuery	☐
Rnd	☐

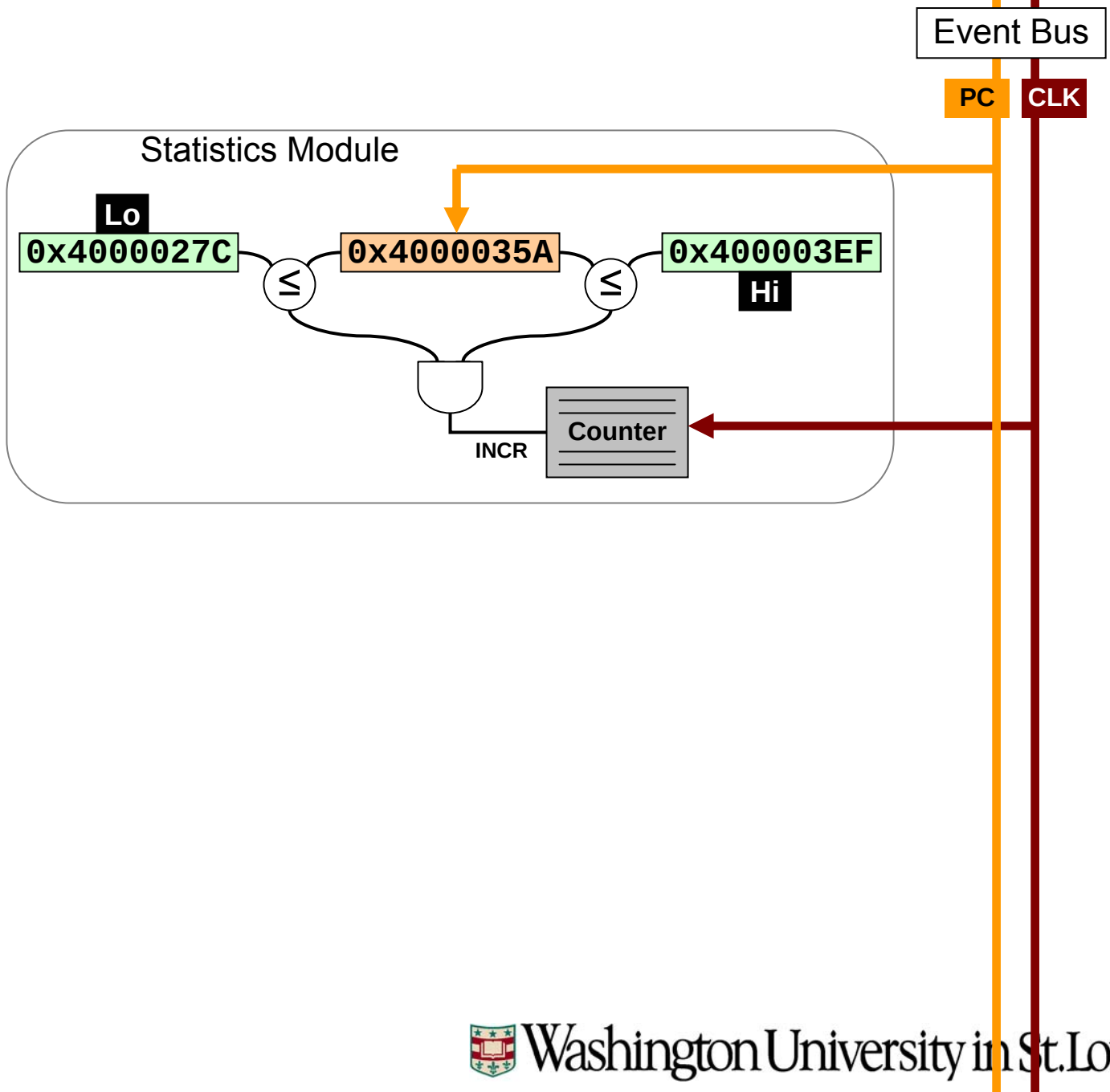
Cycle-accurate profiling

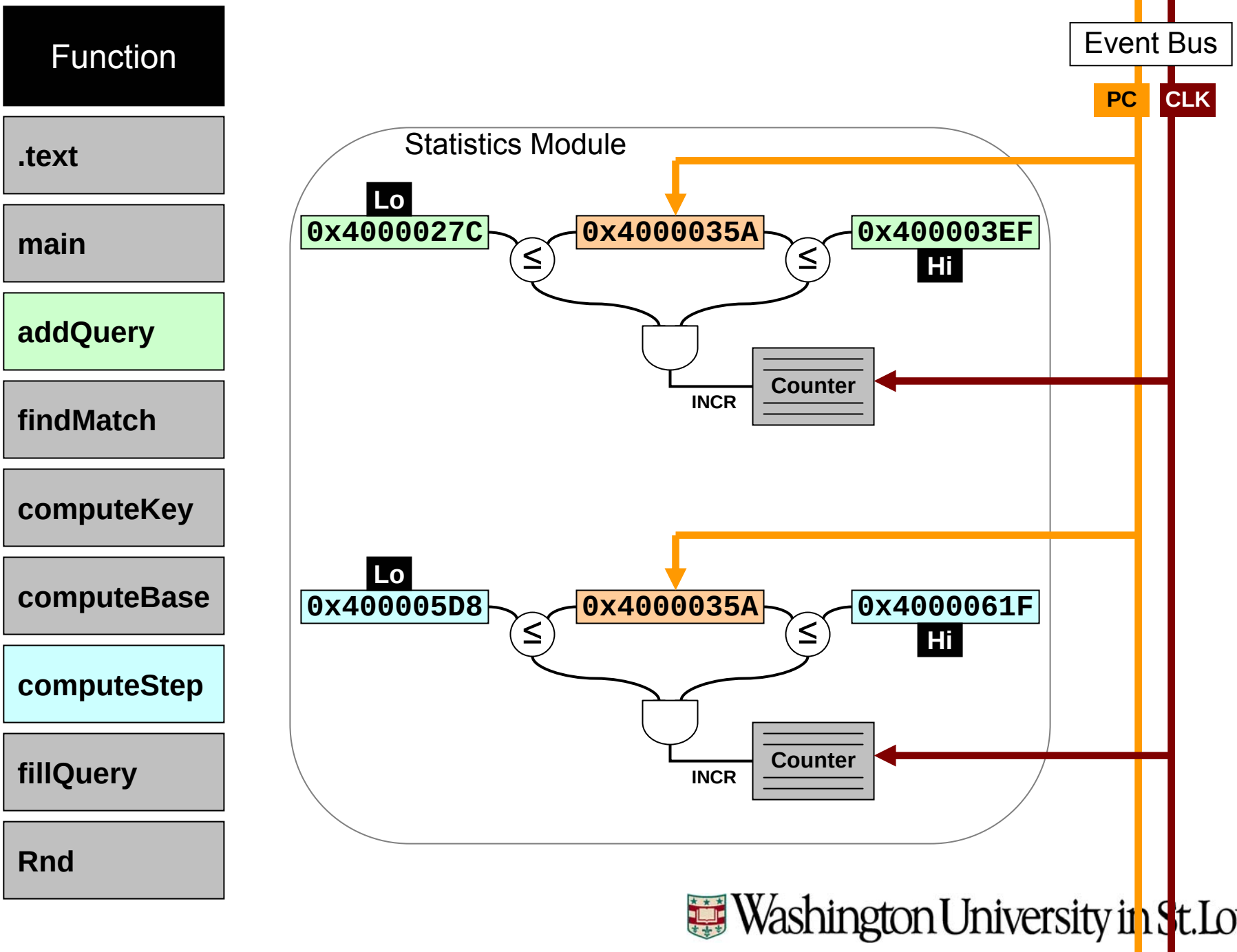
- Choose methods to profile from the user interface

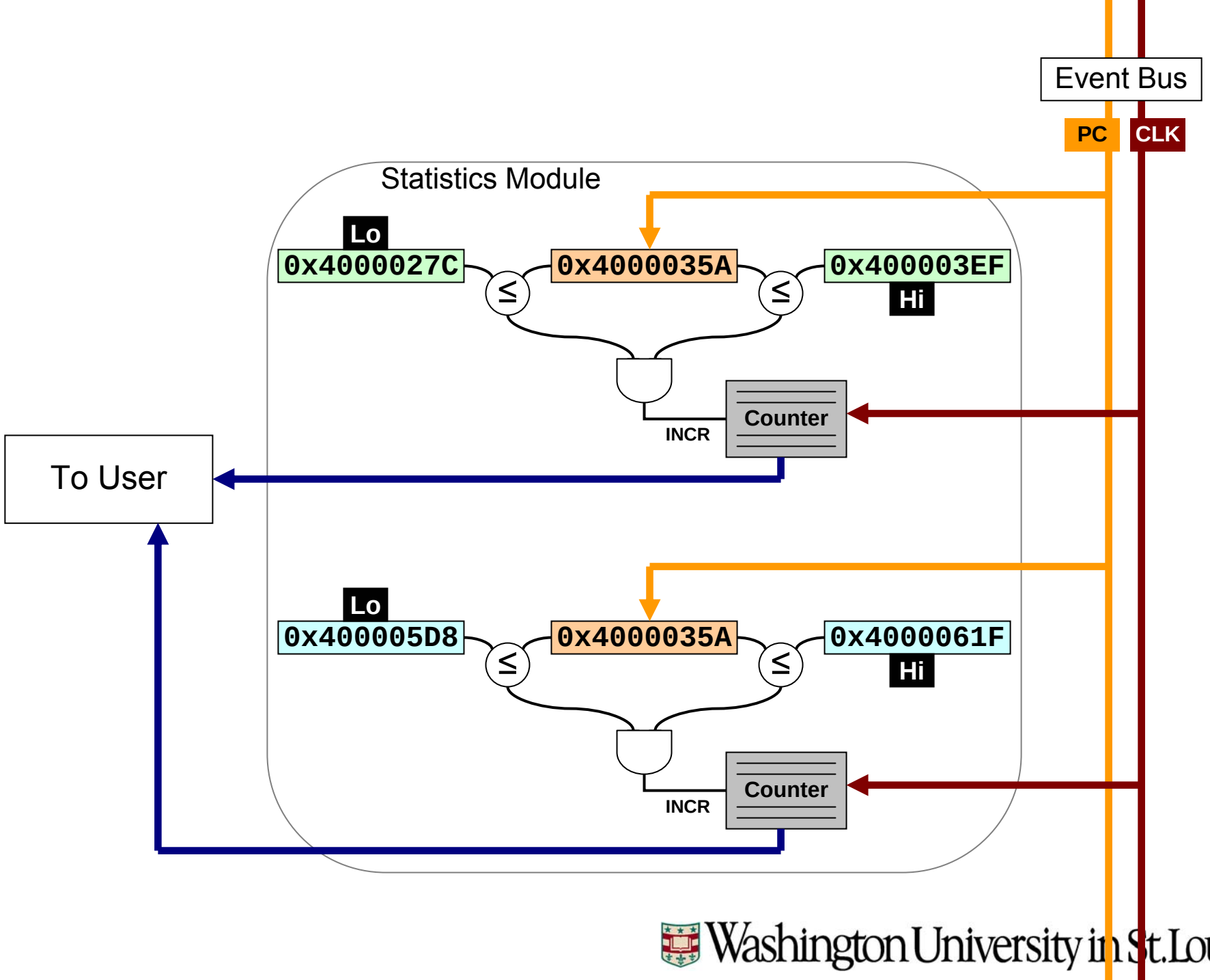
Method	Address Range
.text	
main	
addQuery	Lo 0x4000027C 0x400003EF Hi
findMatch	
computeKey	
computeBase	
computeStep	
fillQuery	
Rnd	


Method
.text
main
addQuery
findMatch
computeKey
computeBase
computeStep
fillQuery
Rnd
Event Bus
PC
CLK
Statistics Module
0x4000035A
Lo
0x4000027C
0x400003EF
Hi

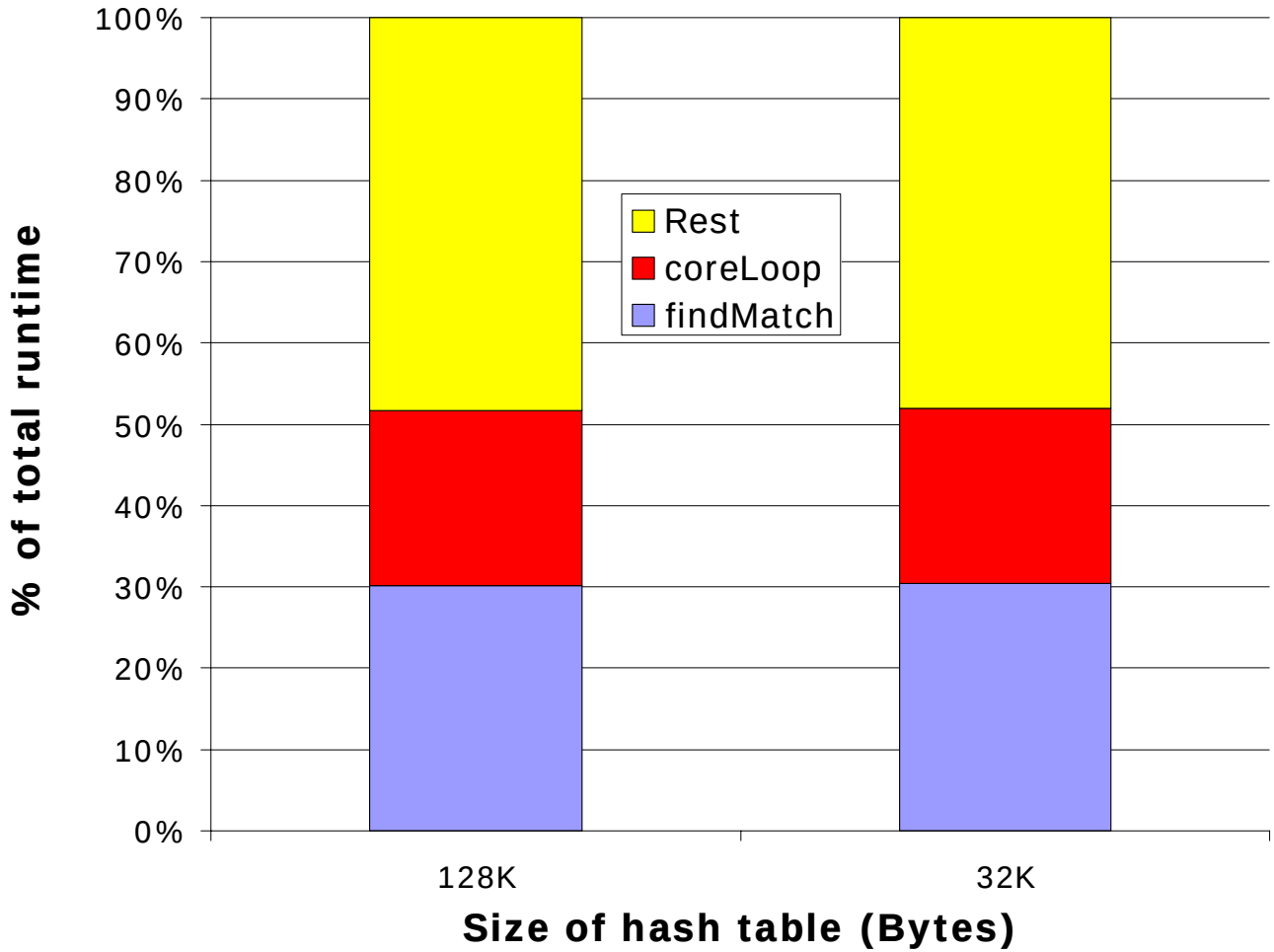
Function
.text
main
addQuery
findMatch
computeKey
computeBase
computeStep
fillQuery
Rnd




Function
.text
main
addQuery
findMatch
computeKey
computeBase
computeStep
fillQuery
Rnd
Event Bus
PC
CLK
Statistics Module
Lo
0x4000027C
≤
0x4000035A
≤
0x400003EF
Hi
INCR
Counter
Lo
0x400005D8
≤
0x4000035A
≤
0x4000061F
Hi
INCR
Counter


Event Bus
PC
CLK
Statistics Module
Lo
0x4000027C
≤
0x4000035A
≤
0x400003EF
Hi
INCR
Counter
To User
Lo
0x400005D8
≤
0x4000035A
≤
0x4000061F
Hi
INCR
Counter

Where is time spent?

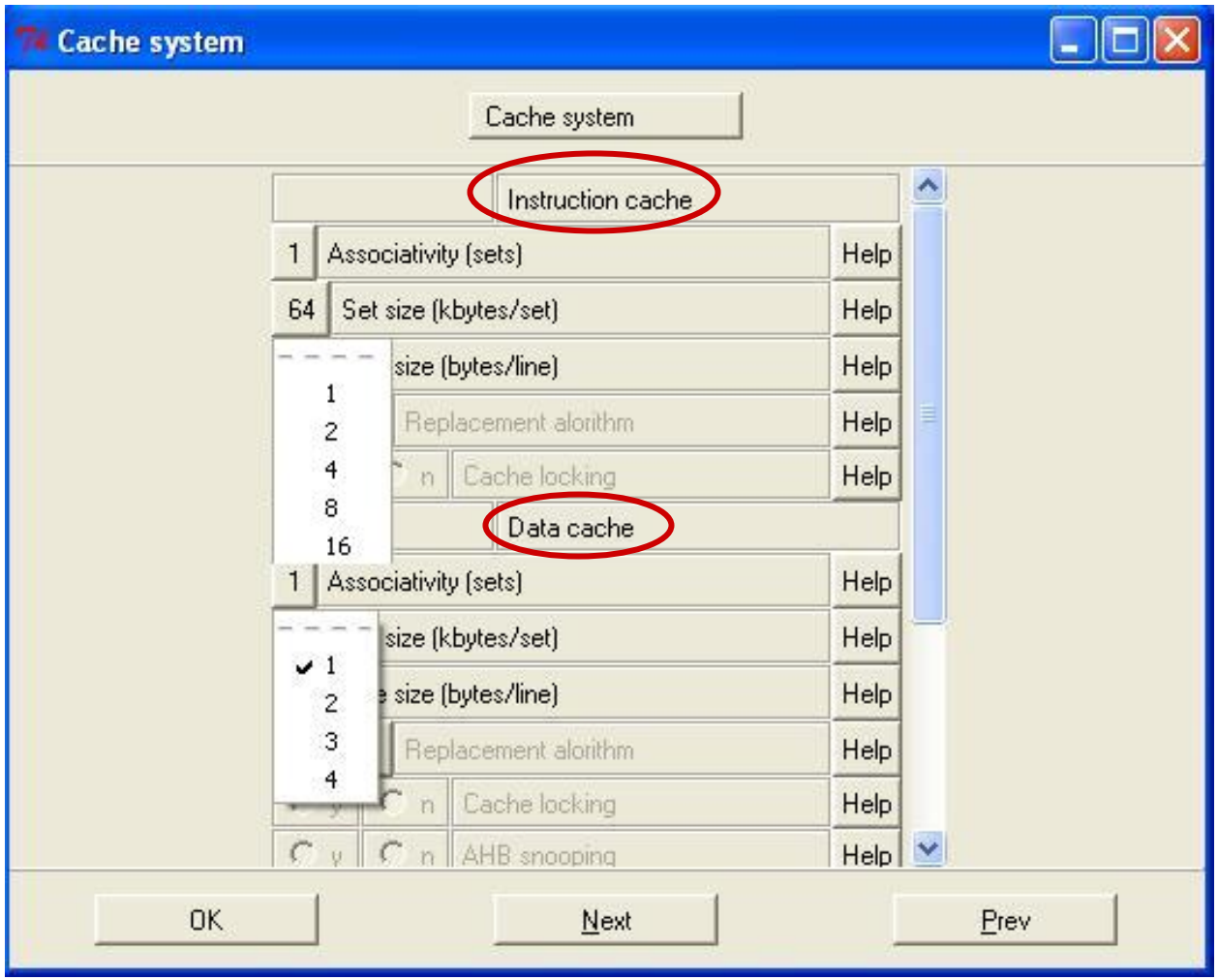


BLASTN biosequence search application

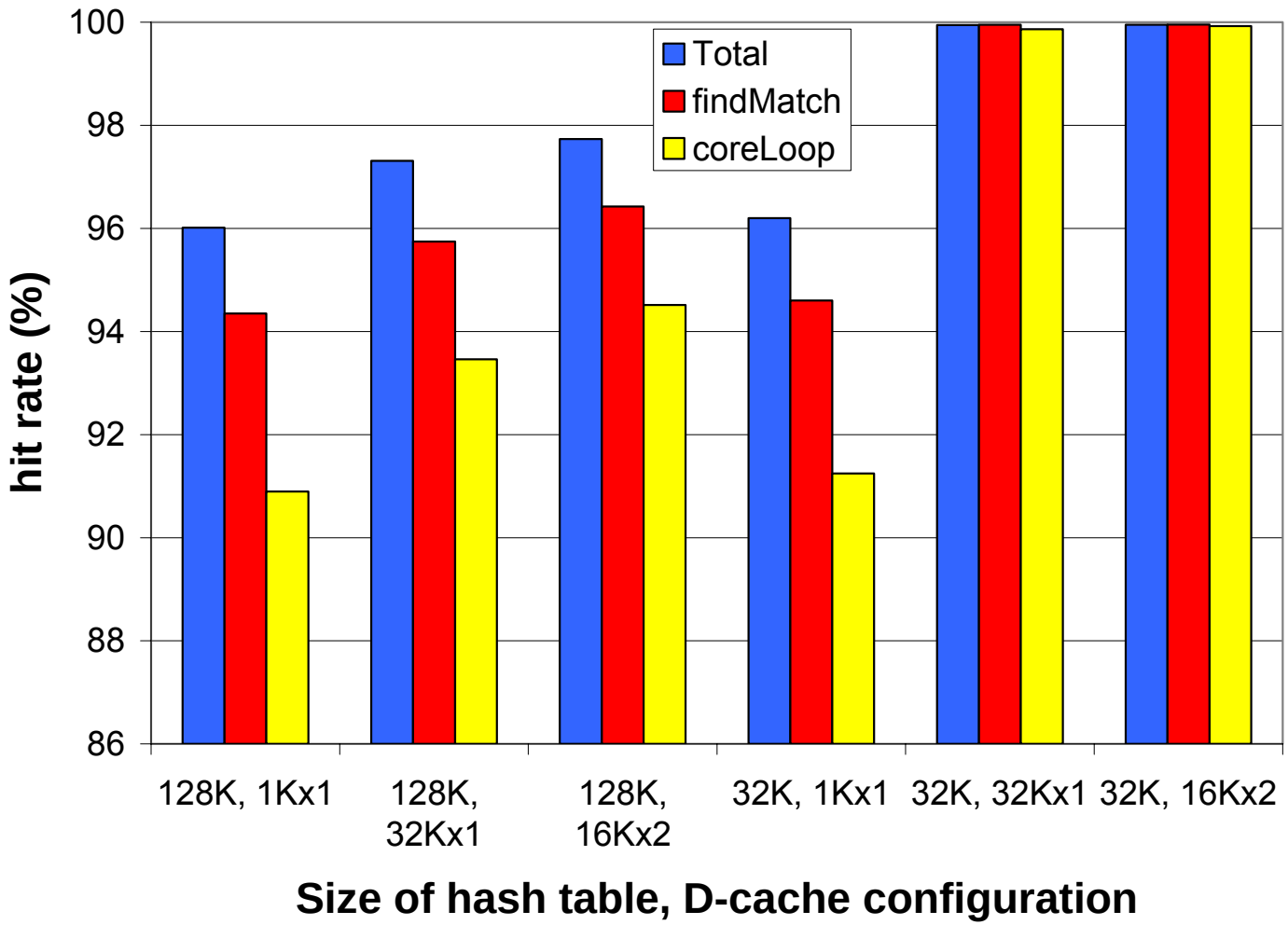
Function	Time / Cycles	Cache Hits / Misses	
		Read	Write
.text	☐	☐	☐
main	☐	☐	☐
addQuery	☑	☑	☑
findMatch	☐	☑	☑
computeKey	☐	☐	☐
computeBase	☐	☐	☐
computeStep	☑	☑	☑
fillQuery	☐	☐	☐
Rnd	☐	☐	☐

Expand to measure cache hits/misses

Measure Several Configurations

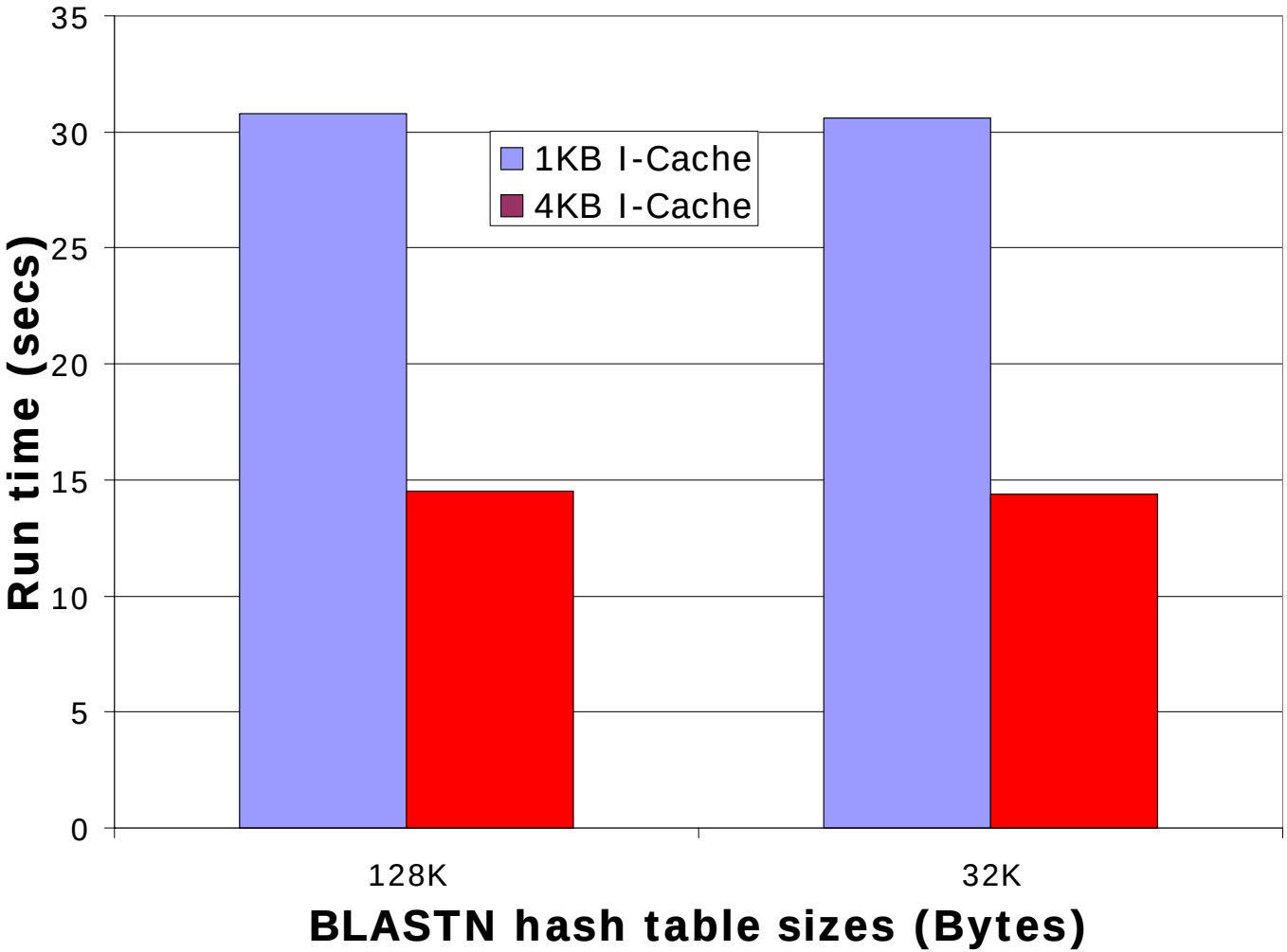


Impact of D-cache Configuration



BLASTN biosequence search application

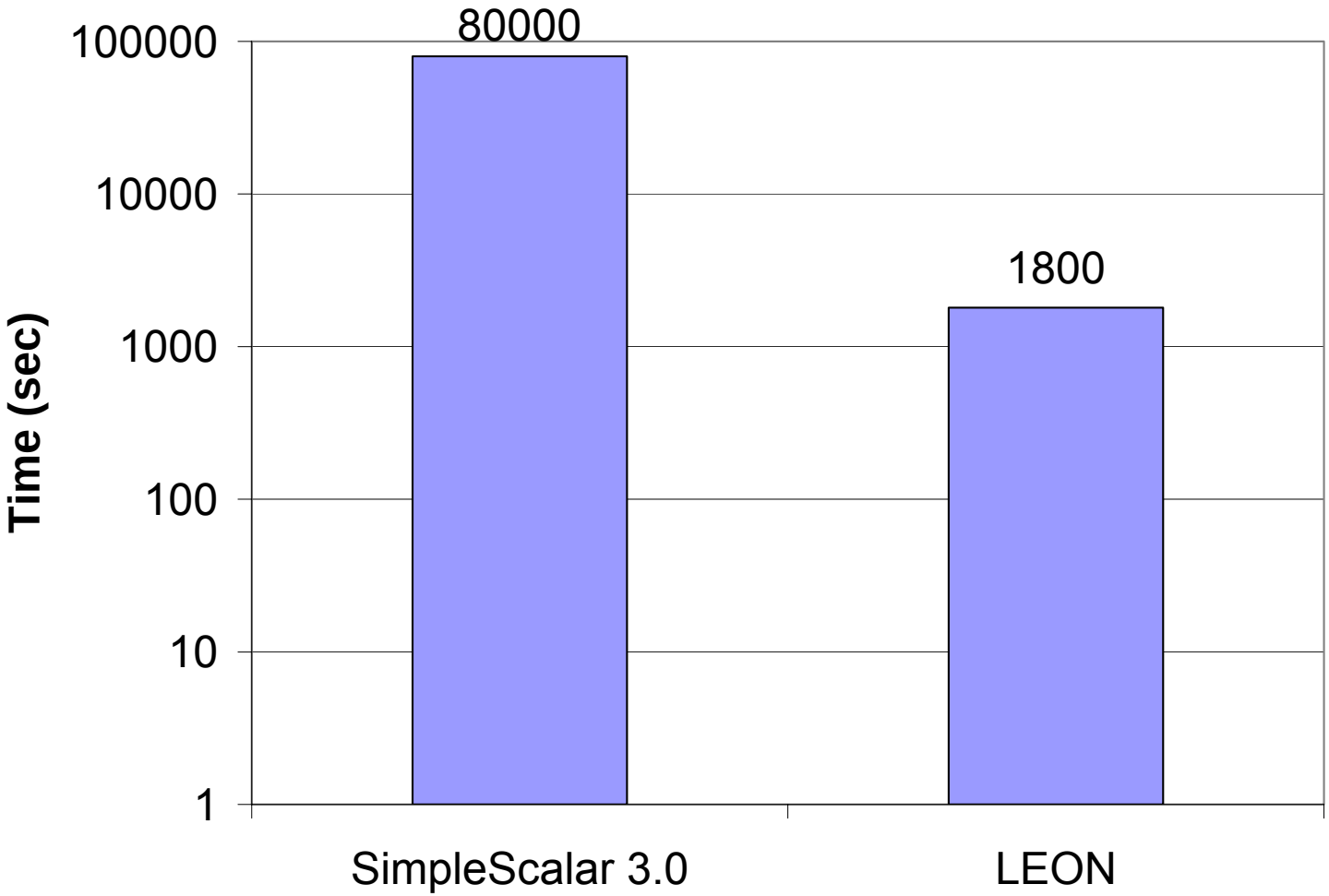
Impact of I-cache Configuration



BLASTN biosequence search application

Function	Time / Cycles	Cache Hits / Misses		Pipeline Stalls	Branch Predict
		Read	Write		
.text	☐	☐	☐	☐	☐
main	☐	☐	☐	☐	☐
addQuery	☑	☑	☑	☐	☐
findMatch	☐	☑	☑	☐	☐
computeKey	☐	☐	☐	☐	☐
computeBase	☐	☐	☐	☐	☐
computeStep	☑	☑	☑	☑	☑
fillQuery	☐	☐	☐	☐	☐
Rnd	☐	☐	☐	☐	☐

Time for Single Run

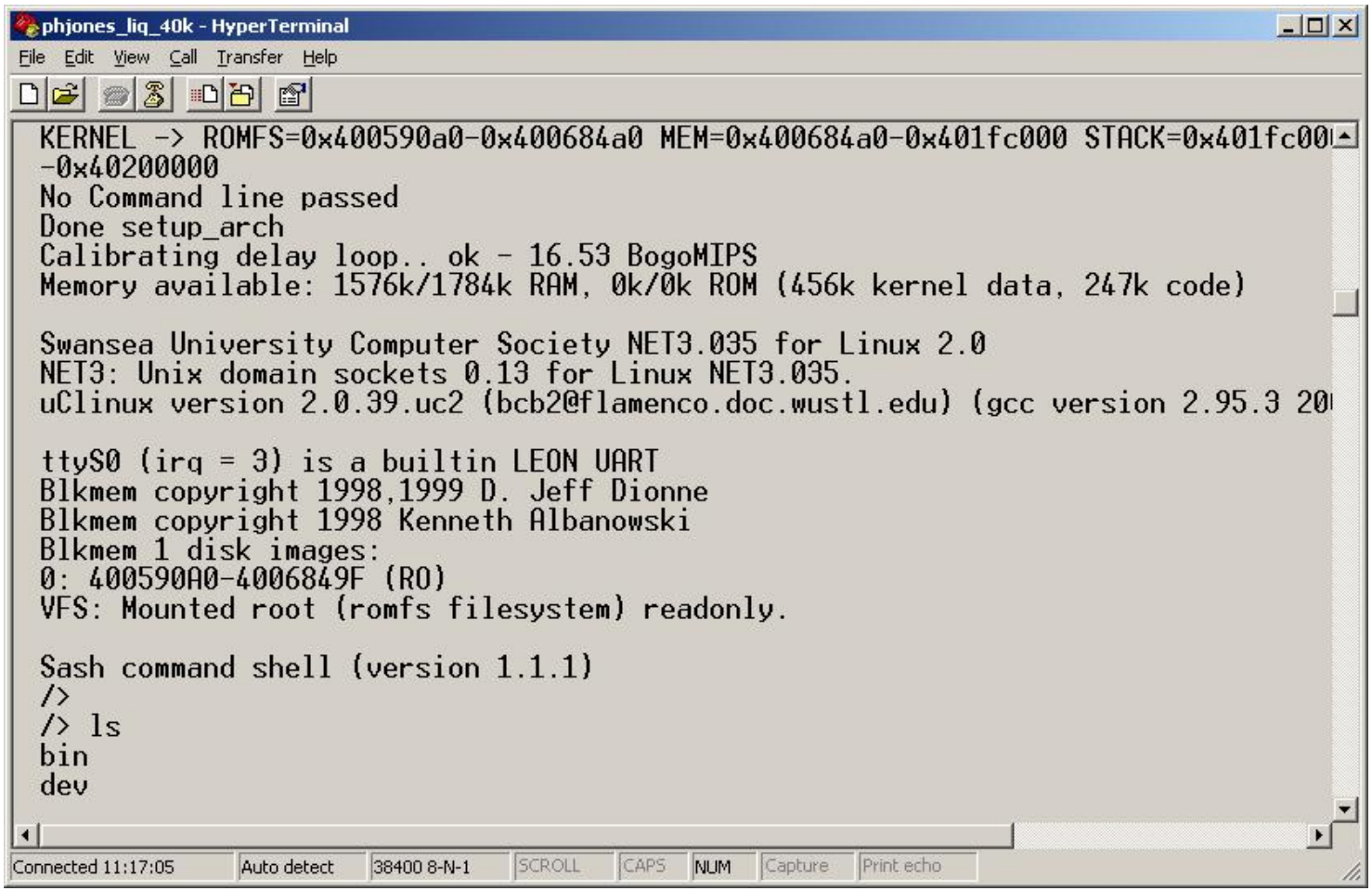


Almost 2 orders of magnitude faster than simulation

Implications of Slow Simulation

- Focus has historically been on measuring the performance of a single thread of a single application
- Real apps are often executed in a multitasking environment
  - Impacts cache behavior
  - Ignores OS (system call) performance
- Liquid architecture system enables direct measurement, including OS

OS Boot Sequence



Summary

- Run-time reconfigurable processors will be available sooner rather than later
- Determining desired configuration is a difficult design task
  - Large search space
  - Depends on accurate performance data
- Liquid architecture system enables direct measurement of performance properties

Current and Future Work

- Evaluation of several arch. design ideas
- Automated search of the design space
- Characterizing performance analysis methods
  - Analytic models
  - Simulation models
  - Direct execution models
- Usable as is for evaluating soft-core procs
- Like to extend to higher-speed procs