Amending Moore's Law for Embedded Applications Panel Discussion

David R. Martinez

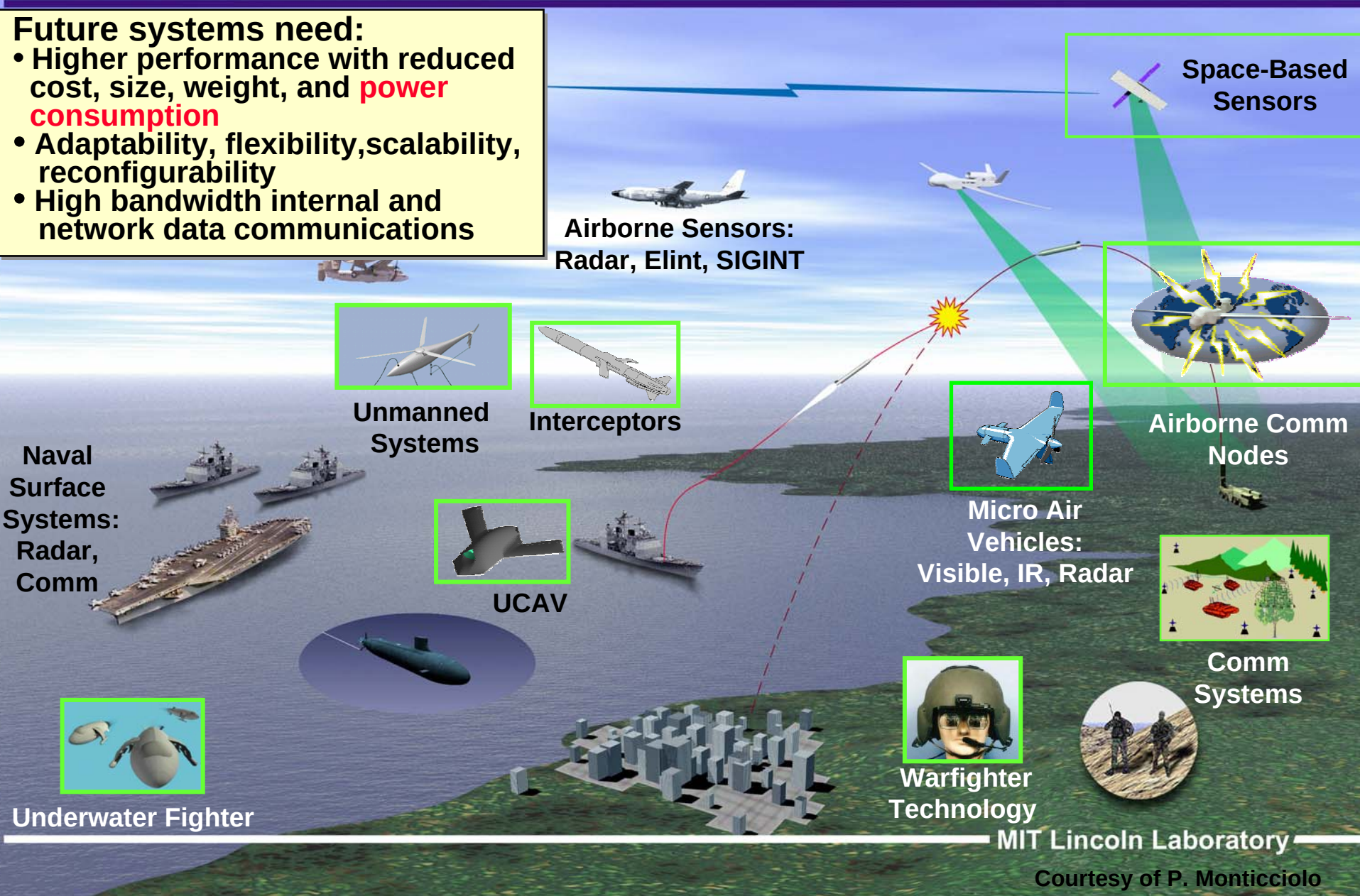
Eighth Annual Workshop on
High Performance Embedded Computing

29 September 2004

This work is sponsored by the Defense Advanced Research Projects Agency under Air Force Contract F19628-00-C-0002. Opinions, interpretations, conclusions and recommendations are those of the author and are not necessarily endorsed by the United States Government.

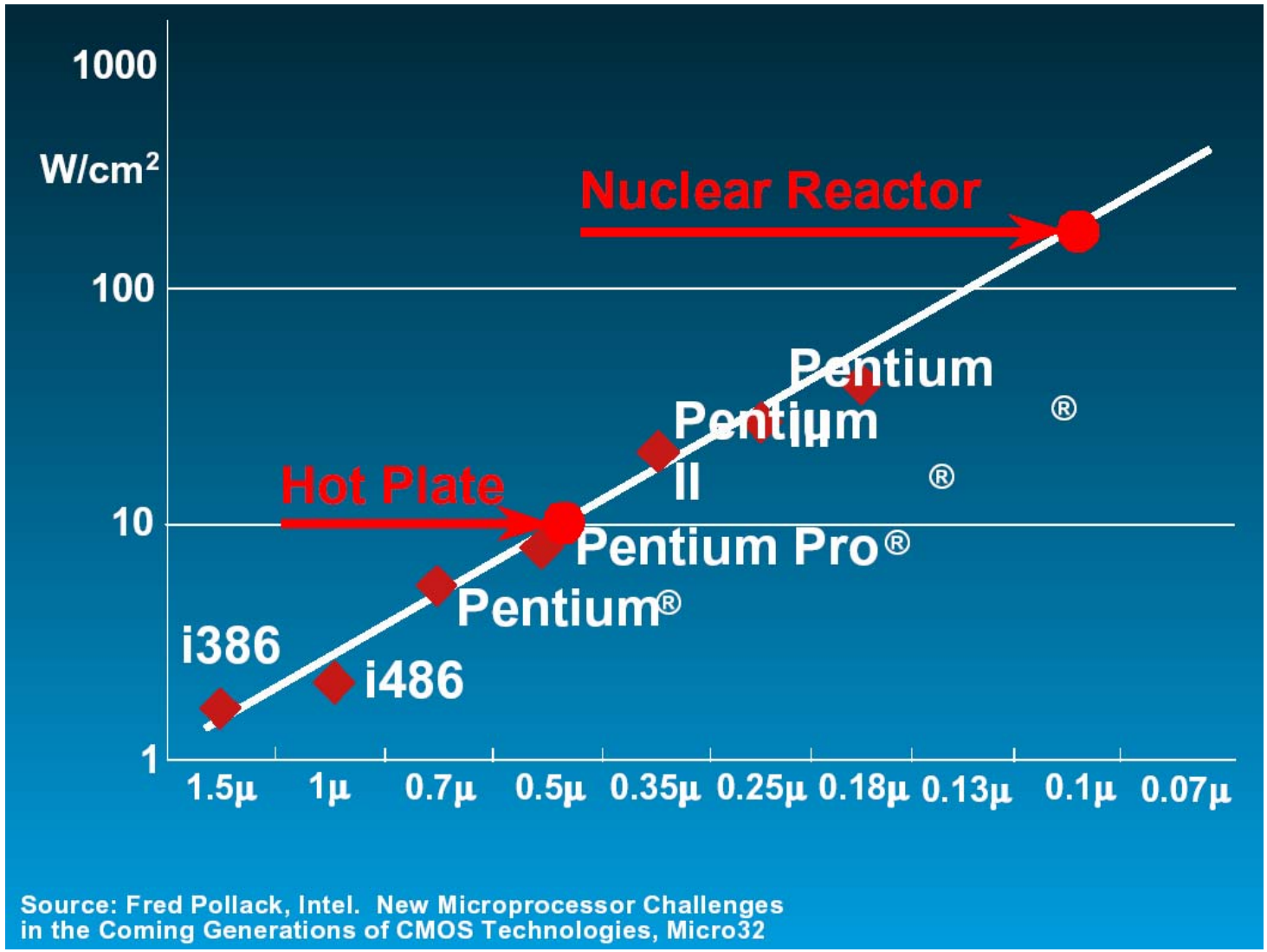
DoD Embedded Processing Applications

Future systems need:
- Higher performance with reduced cost, size, weight, and power consumption
- Adaptability, flexibility,scalability, reconfigurability
- High bandwidth internal and network data communications



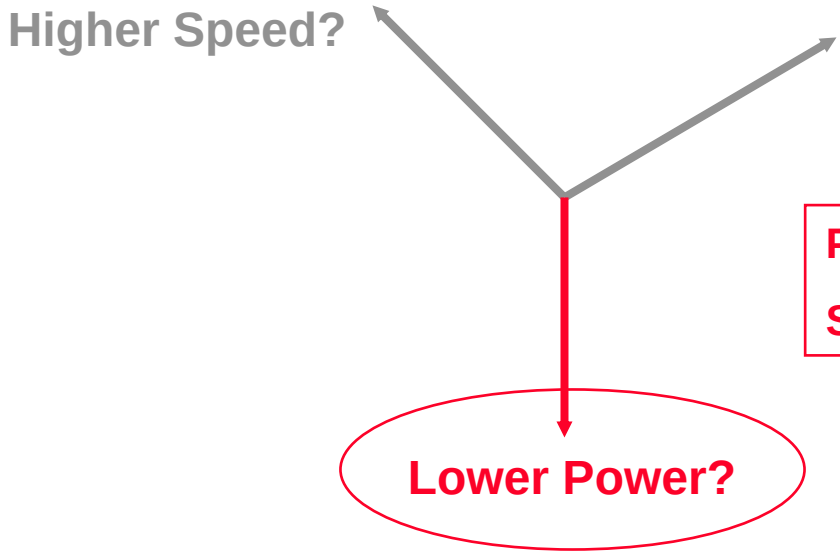
Courtesy of P. Monticciolo

Power Density: The Fundamental Problem



Courtesy of C.Keast

Prognosis For Moore's Law Benefits



Pentium 4 (90nm): ~80 W/cm^2

Stovetop: ~10 W/cm^2

Past

Supply voltage (V) scales as 1/s

Capacitance (C) scales as 1/s

Energy per op scales as $CV^2 \propto 1/s^3$

⇨Voltage scaling from 5V to 1V accounts for 25X reduction in power, just by itself

Future Issues

Only 2x voltage scaling planned (1V now to ~0.5V in 2016)

⇨ Scaling energy per op is critical to long endurance battery powered systems and to supercomputers (getting power in and heat out)

Courtesy of D. Shaver