Hardware Benchmark Results for An Ultra-High Performance Architecture for Embedded Defense Signal and Image Processing Applications

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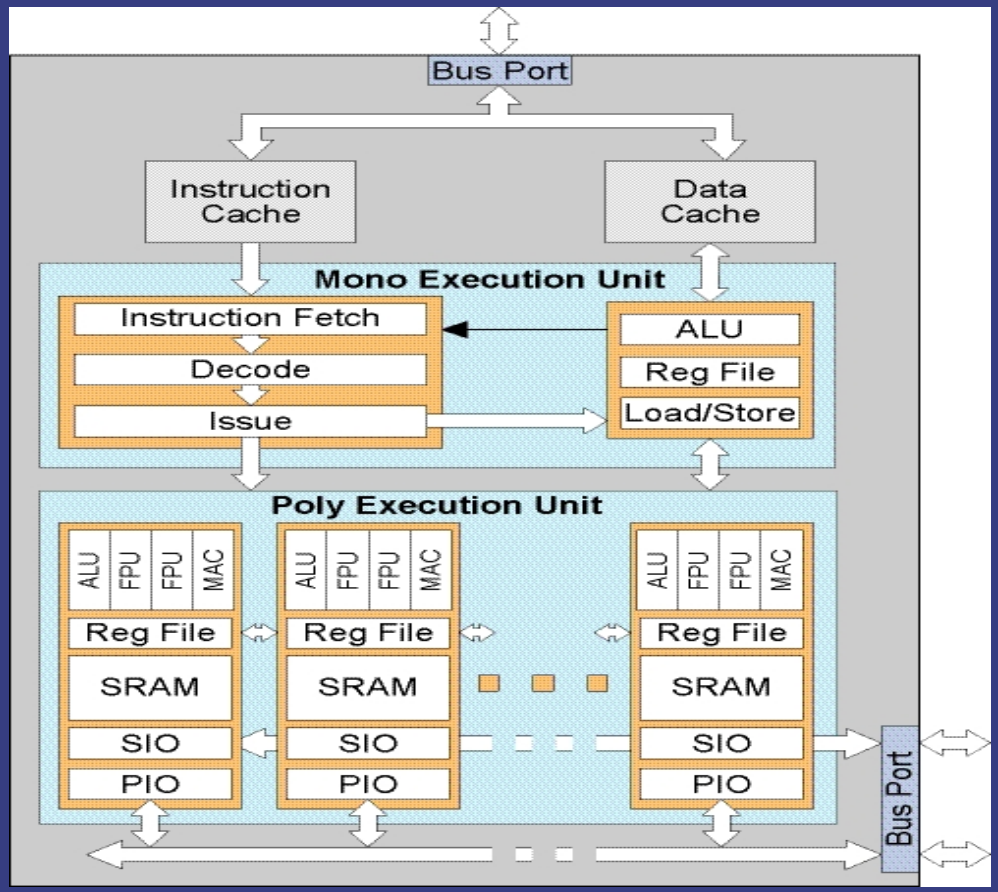
Architecture

- *ClearSpeed's* Multi Threaded Array Processor Architecture – MTAP



Applications

✦ Power Comparison Results

(Table presented at HPEC 2003)

Processor	Clock	Power	FFT/sec /Watt	PC/sec/ Watt
Mercury PowerPC 7410	400 MHz	8.3 Watts	3052	782.2
World*Scape*/ *ClearSpeed* 64 PE Chip	200 MHz	2.0 Watts**	56870	24980
Speedup	----	----	18.6 X	31.9 X

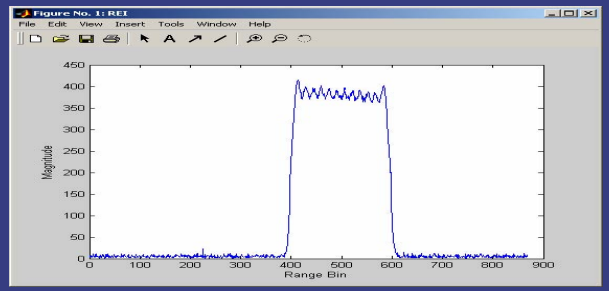
** 2.0 Watts was the worst case result from Mentor Mach PA Tools.

Actual Measured Hardware Results < 1.85 Watts

HPEC 2003 Cycle Accurate Simulations were validated on actual hardware. Results matched to within 1%.

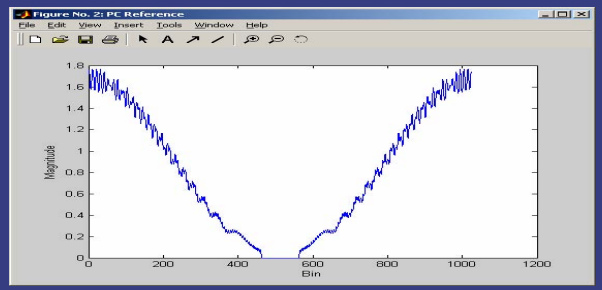
Benchmark

•Pulse Compression Input (MatLab)



- 1 KHz PRF (1ms PRI)
- 20 MHz sampling rate
- 870 samples
- Echo
  - 10 us pulse
  - LFM chirp up
  - 200 samples

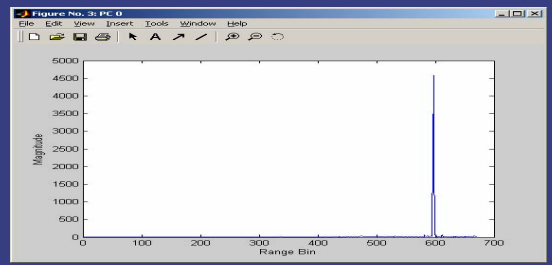
•Pulse Compression Reference (MatLab)



- Frequency Domain Reference
- 10 us
- LFM chirp up
- 1024 samples
- Hamming weighting
- Bit-reversed to match optimized implementatio

•Pulse Compression Output (MatLab)

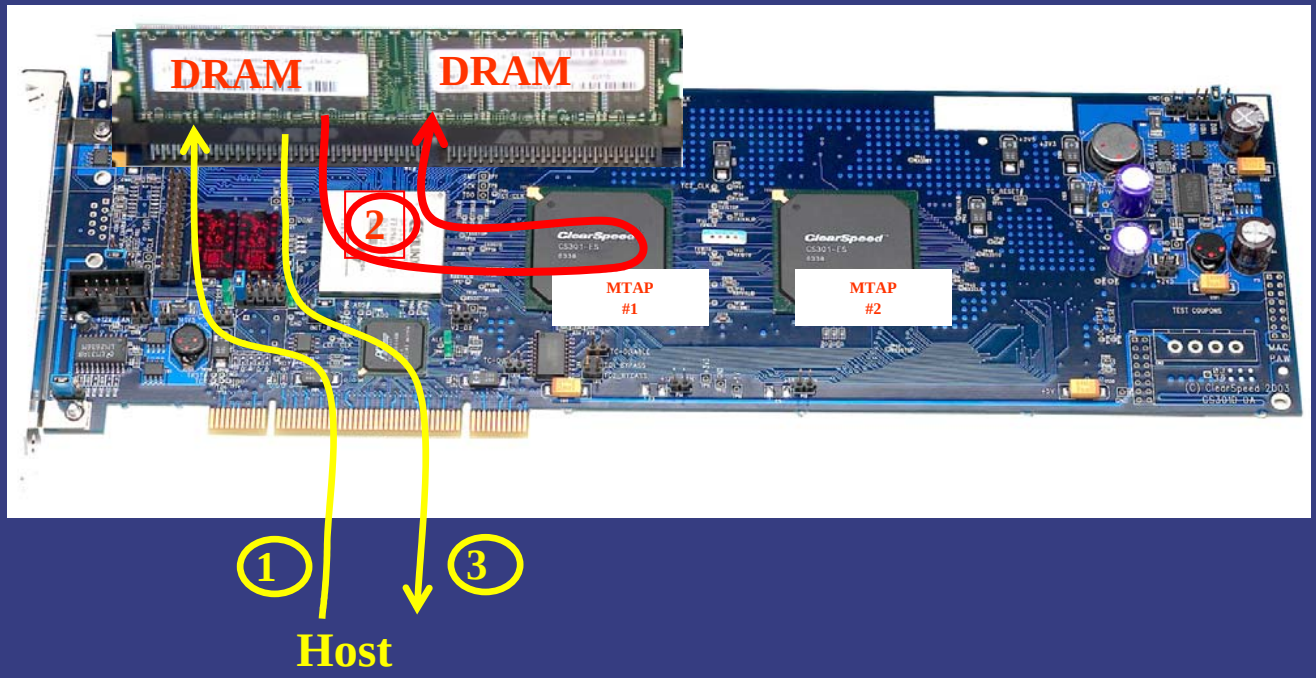
- 671 samples out of PC



Benchmark

Benchmark Measurements:

Validate Pulse Compression performance with hardware and with data flowing from and to external DRAM (1 MTAP processor)



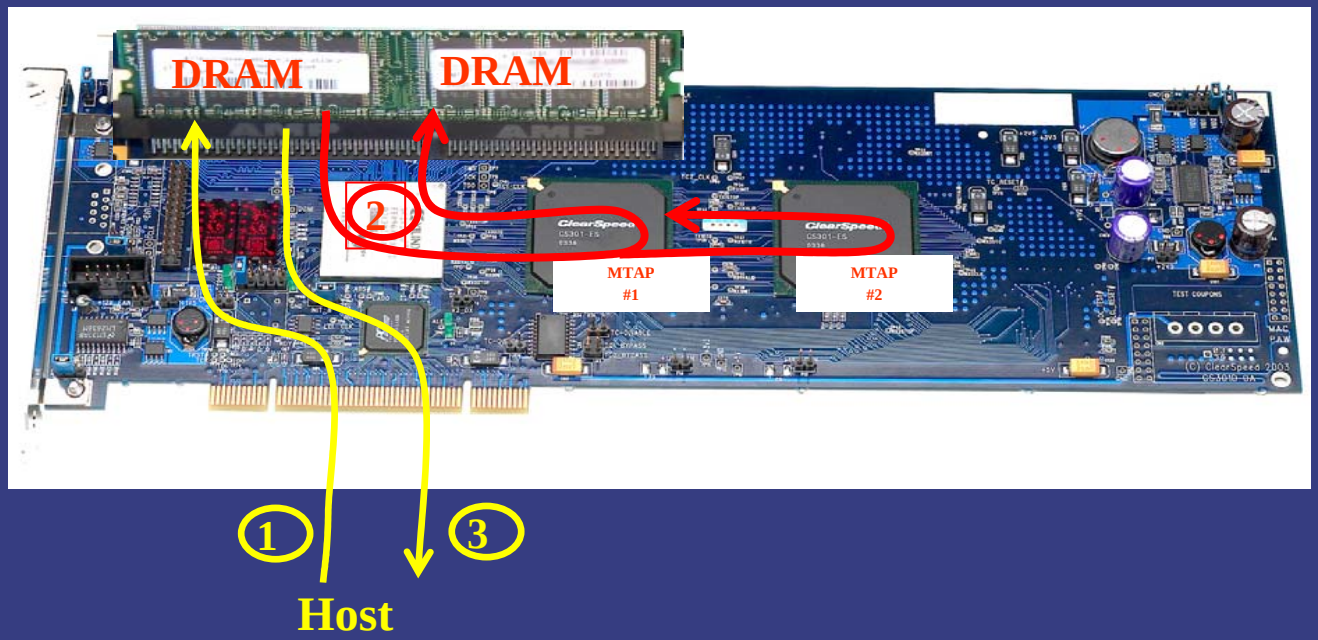
1) Input Data and reference Function loaded from Host onto DRAM
2) Data input from DRAM to MTAP #1, processed, and output into DRAM
3) Results returned to Host for display

Benchmark

Benchmark Measurements:

Validate Pulse Compression performance with hardware and with data flowing from and to external DRAM

(Average Performance across 2 MTAP processors)



1) Input Data and reference Function loaded from Host onto DRAM

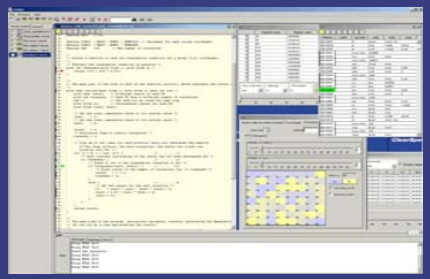
2) Data input to MTAP #1 and (via MTAP #1) to MTAP #2, processed, and output (via MTAP #1) into DRAM

3) Results returned to Host for display

Summary

Hardware validation of HPEC 2003 results to within 1%

World-class radar processing benchmark results



Optimized Pulse Compression functions modified using COTS SDK and integrated onto Host platform

Wide Ranging Applicability to DoD/Commercial Processing Requirements

- **VSIPL Core Lite Libraries under development**

Application Areas

- Image Processing
- Signal Processing
- Compression/De-compression
- Encryption/De-cryption
- Network Processing
- Search Engine
- Supercomputing Applications