

# Dynamo: A Runtime Codesign Environment

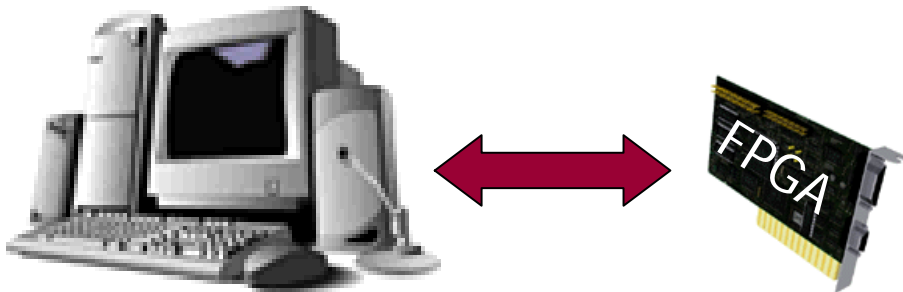
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On this Environment:



Which implementations to use?

How to minimize overall latency?

When to use FPGA?

How to change the pipeline or interfaces dynamically?

Run this pipeline:





# Goals

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Predict pipeline latency accurately:

Model includes all overhead costs of using the FPGA

Implement low latency solutions:

Problem space quickly searched

Build and execute pipelines at runtime:

User is not impacted

# Dynamo System Overview

**Input:** The pipeline specification, an image, and a device name

**Output:** Results from executing pipeline on the image

**Libraries:** ipBLOC

**Model:** Pipeline Assignment

