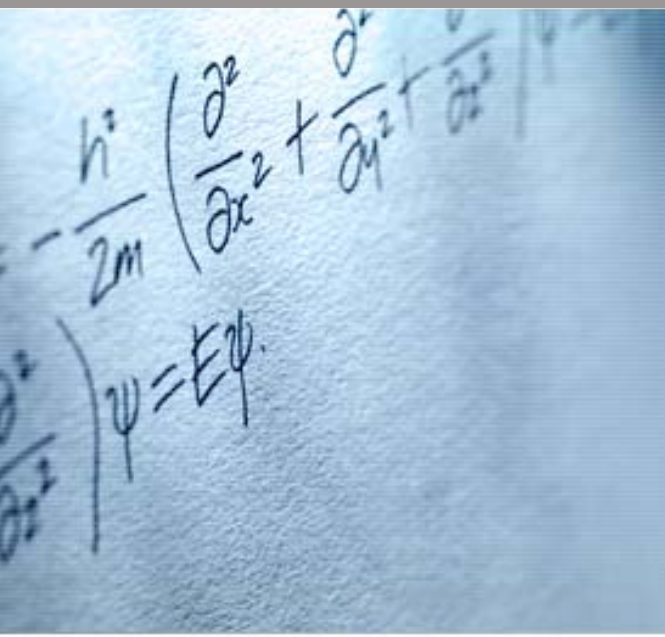
ClearSpeed



ClearSpeed's CS301:
The World's First Commercially-Available Stream Processor

Architecture, Algorithms and Benchmark Results

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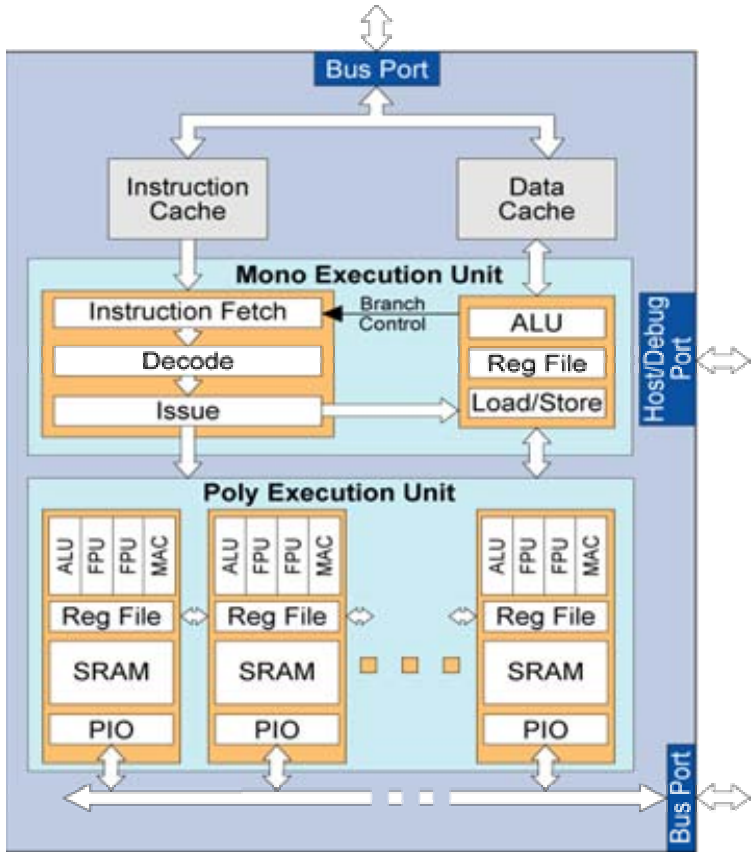
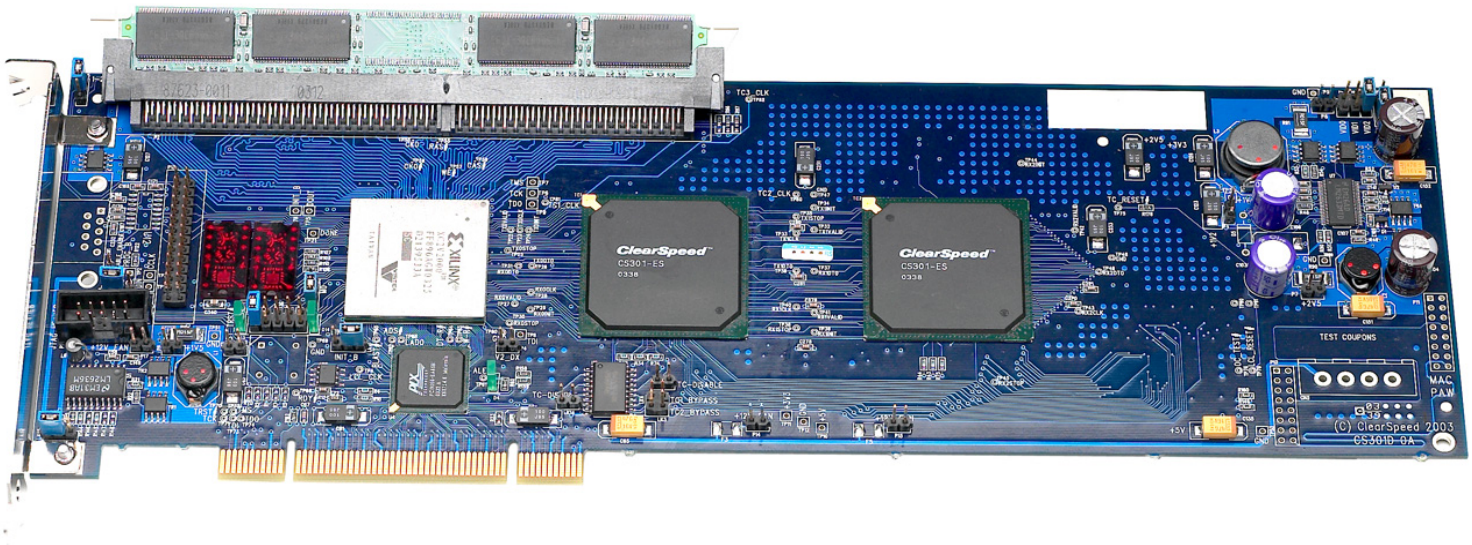
A Better Approach: ClearSpeed's CS301 Processor



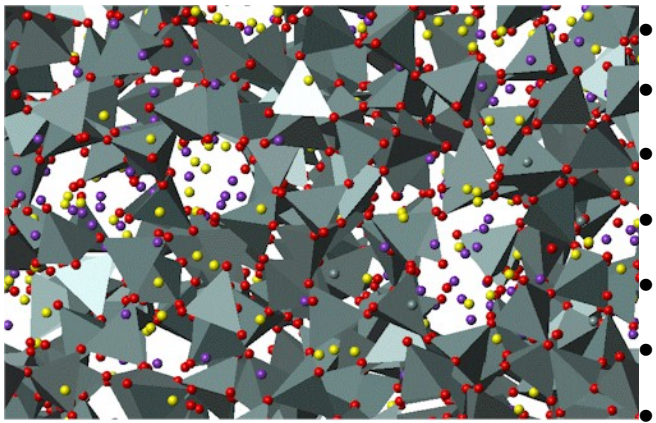
- Multi-threaded Array Processing
  - Programmed in high-level languages
  - Hardware multi-threading
    - Enables simultaneous data streaming and computation for latency tolerance
  - Run-time extensible instruction set
- Array of Processors Elements
  - PEs are VLIW cores
  - Flexible data parallel processing
  - Built-in PE fault tolerance, resiliency
- High performance, low power
  - 10 GFLOPS/Watt
- Multiple high bandwidth I/O channels

CS301 Based Development Board



- 50 GFLOPS peak @ 10W maximum
- 200K FFTs/s (1K complex single precision IEEE754)
- Up to 1GB DRAM for local processing
- Single slot width full-size PCI card
- In evaluation use since early 2004

ClearSpeed AWE Joint Investigation

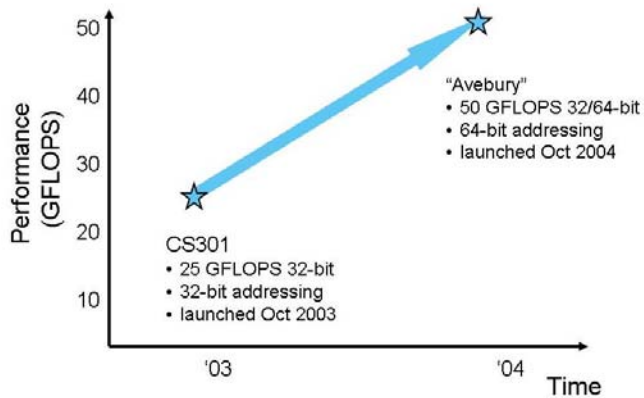


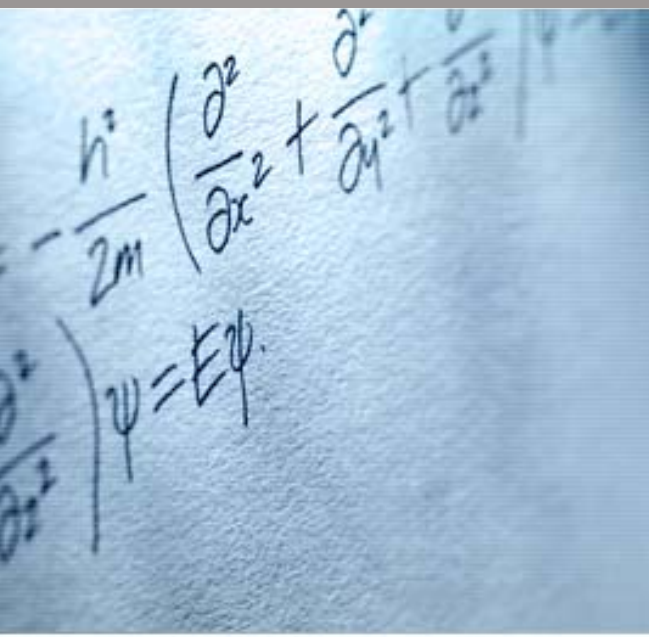
Chemistry codes: DLPOLY (Molecular Dynamics)

- Owned by UK Daresbury Laboratory
- Widely used within AWE, also academia & industry
- 91% of CPU time in 5 small routines
- One calls the other 4 to compute forces on all atoms
- Forces called once per time step
- Small amount of data returned by forces from CS to host
- Calculation for each atom is independent

Matrix Multiply Benchmark (SGEMM)

- CS301 single precision code started at ~20% efficiency
- AWE/CS code restructuring gave 12 GFLOPS – 47%
- Performance verified by AWE on CS301 hardware
- “Avebury” significantly increases this performance





Extremely Cool, Extremely Fast

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