Sparse Linear Solver for Power System Analysis using FPGA

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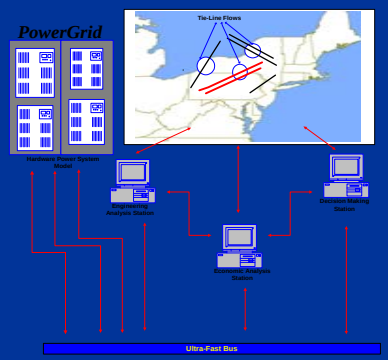

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Goal & Approach

- To design an embedded FPGA-based multiprocessor system to perform high speed Power Flow Analysis.
- To provide a single desktop environment to solve the entire package of Power Flow Problem (Multiprocessors on the Desktop).
- Solve Power Flow equations using Newton-Raphson, with hardware support for sparse LU.
- Tailor HW design to systems arising in Power Flow analysis.

Results

- Software solutions (sparse LU needed for Power Flow) using high-end PCs/workstations do not achieve efficient floating point performance and leave substantial room for improvement.
- High-grained parallelism will not significantly improve performance due to granularity of the computation.
- FPGA, with a much slower clock, can outperform PCs/workstations by devoting space to hardwired control, additional FP units, and utilizing fine-grained parallelism.
- Benchmarking studies show that significant performance gain is possible.
- A 10x speedup is possible using existing FPGA technology