Reconfigurable Computing
MONARCH/MCHIP
High Efficiency Embeddable TeraFlops Polymorphous Computing Architecture

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Raytheon / USC-ISI

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MOrphable Networked micro-ARCHitecture

Exogi

MONARCH System on a Chip

RISC, DRAM, Computing Array, Streaming I/O

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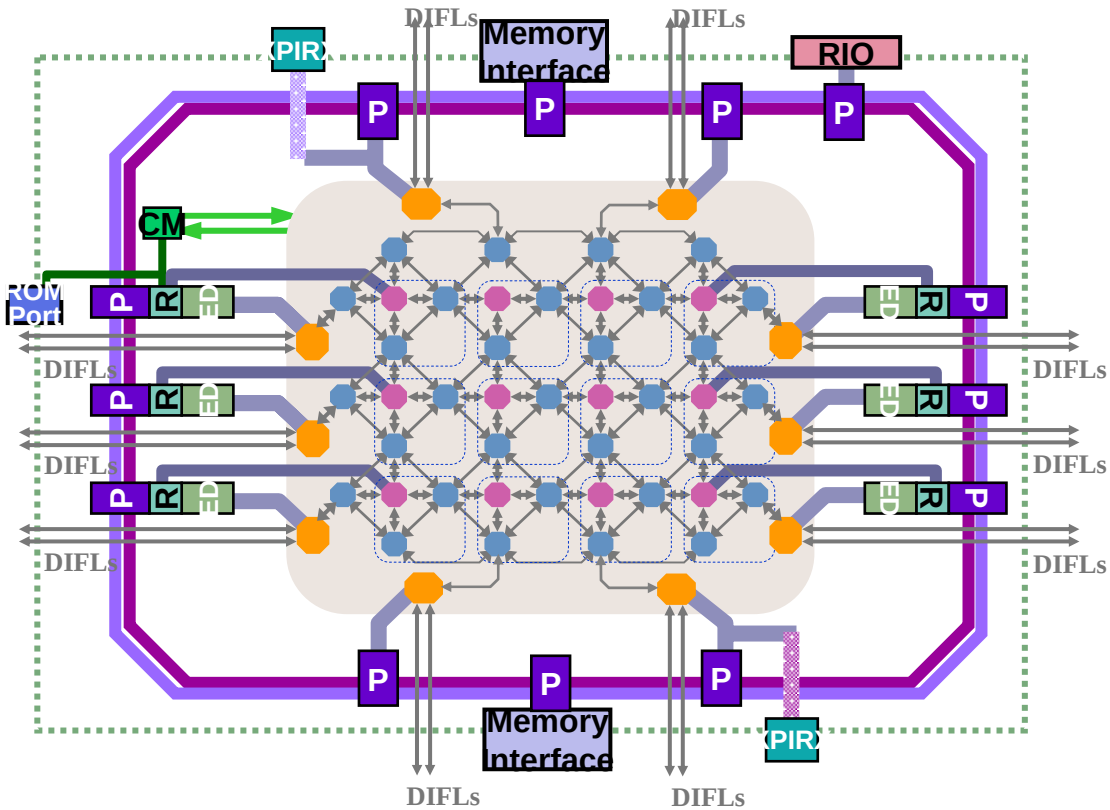
Space and Airborne Systems



- Alternative to ASICS or custom hardware
- Demonstrated for RADAR, COM, EO
- Late algorithm freeze – retains programmability
- Energy efficiency: 3-6 GFLOPS/W

- Polymorphous Architecture
- Multiple programming modes
  - Reconfigurable, streaming DF
  - RISC scalar
  - RISC SIMD (Altivec like)
- 6 RISC processors
- Reconfigurable Computing
  - 96 adders fixed and float
  - 96 multipliers
  - 124 dual port memories
  - 248 address generators
- 12 MBytes on chip DRAM
- 14 DMA engines
- RapidIO interface
- 20 DIFL ports (1.3 GB/s ea)
- Power 8-50 W (nominal)
- Throughput 64 GFLOPS peak

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Application Development Environment & Workstation

DARPA

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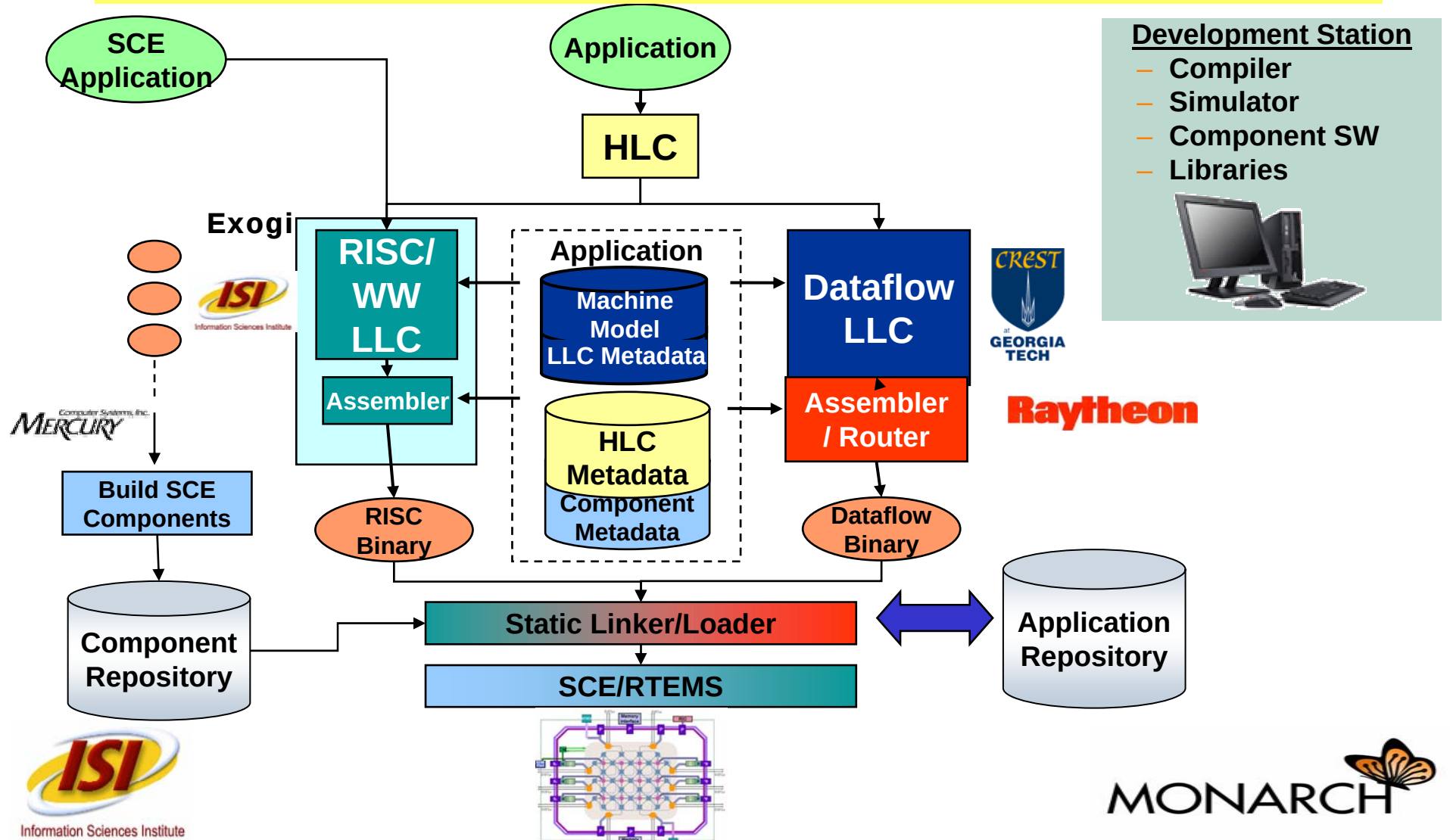
Space and Airborne Systems

Multiple Computing Modes adapt to application needs:
1) RISC Scalar, 2) Wide Word, 3) Reconfigurable Data Flow



MONARCH Performance on Lincoln Lab Benchmark Suite

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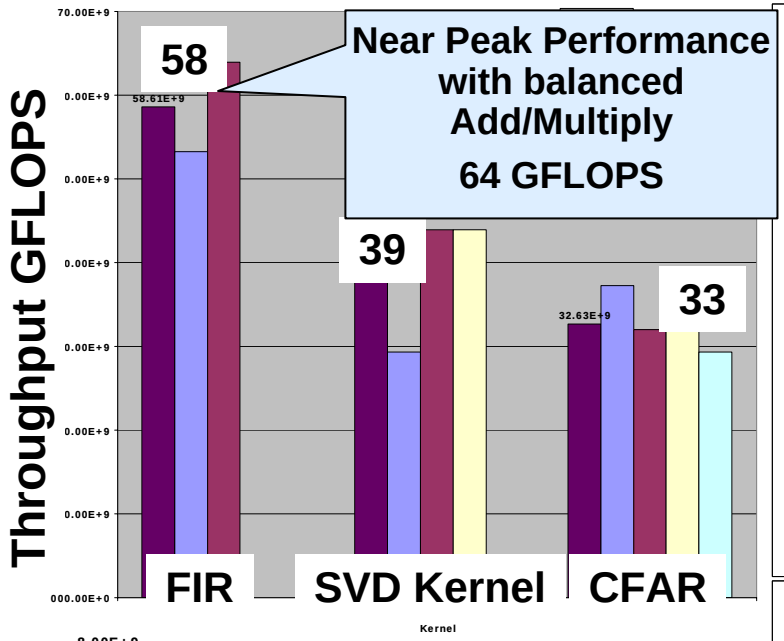

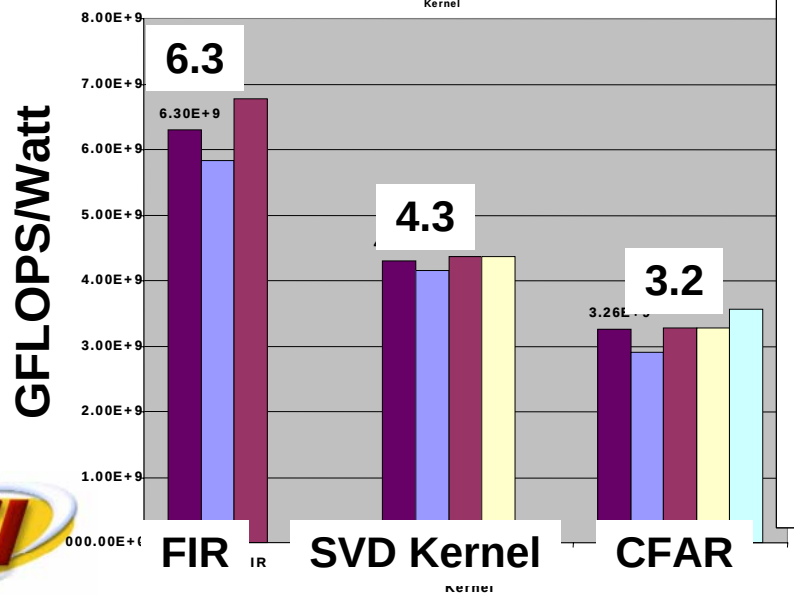

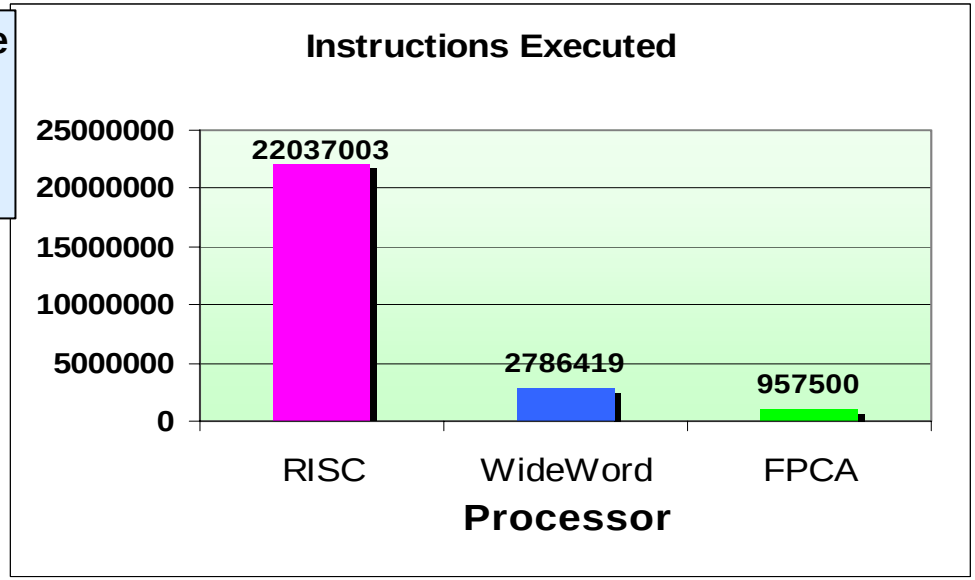

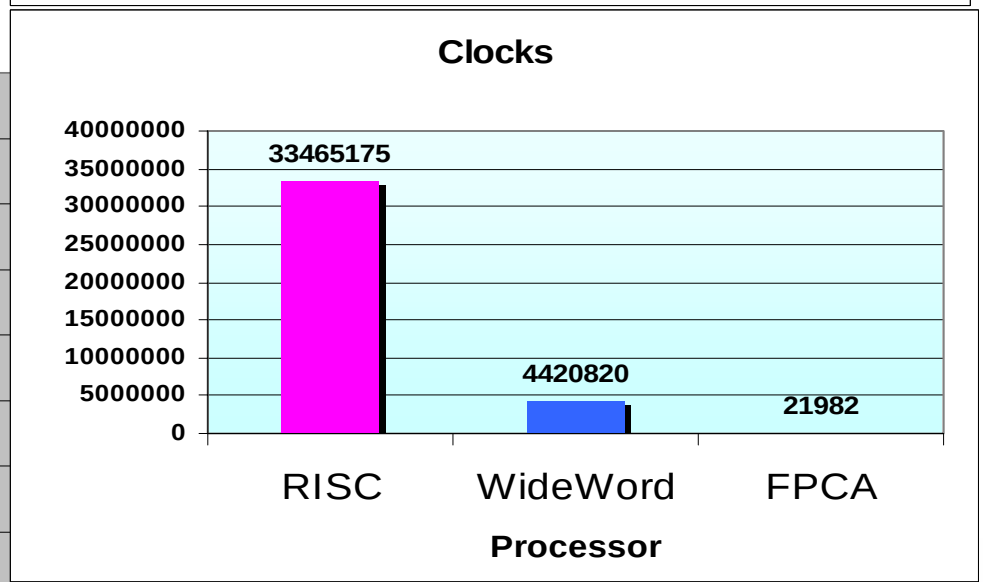

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