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Processing Challenges in Shrinking HPEC Systems into Small Platforms

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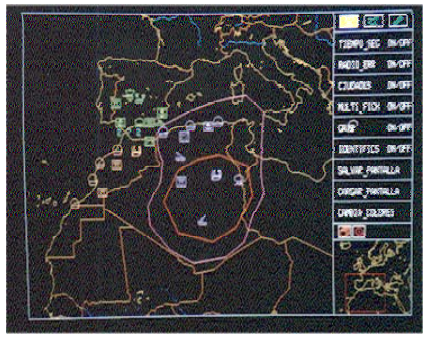
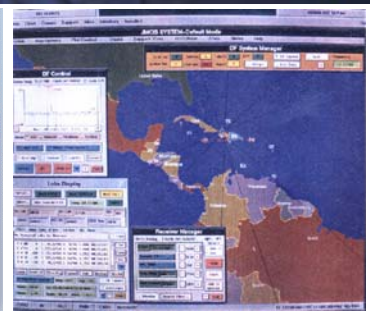
The Ultimate Performance Machine

Target Applications

- COMINT/ESM
- Software Radio
- Radar
- ELINT/ESM/RWR
- EO/IR Imagery

… and other HPEC challenges, such as ATR, to reduce sensor communication bandwidth/latency needs





Target Platform Types

- UAVs
- Helicopters
- Man-pack/Brief-case
- Small Vehicle
  - e.g., Humvee
- Manned aircraft
  - e.g., ARC-210 radio
- Airborne Pods


Predator


SH60


Prophet


JSF


F-18 (POD)

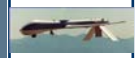

F-16


RAPTOR


Gripen


Litening Pod

Platforms with SWAP Constraints - UAVs

UAV	Global Hawk	Pred-ator B	Heron A	Hunter	Eagle Eye	Fire-Scout	Sentry	Dragon Warrior	Dragon Eye
Picture									
Length (ft)	44.4	36	26	22	17	23	8.4	10	3
Wingspan (ft)	116	66	54	29	17	20	12.8	9	3.8
Height (ft)	14	9.5	5.9	5.6	5.5	9.5	4	5	1
Payload Weight (lbs)	1000	800	550	250	200	200	75	35	5
Max Altitude (ft)	65k	50k	25k	15k	20k	20k	15k	4k	1.2k
Sensors	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR	EO/IR	EO/IR
Endurance (hrs)	36	36	36	10	5	4	3	3	1
Max Airspeed (kts)	320	220	120	100	220	120	100	70	35

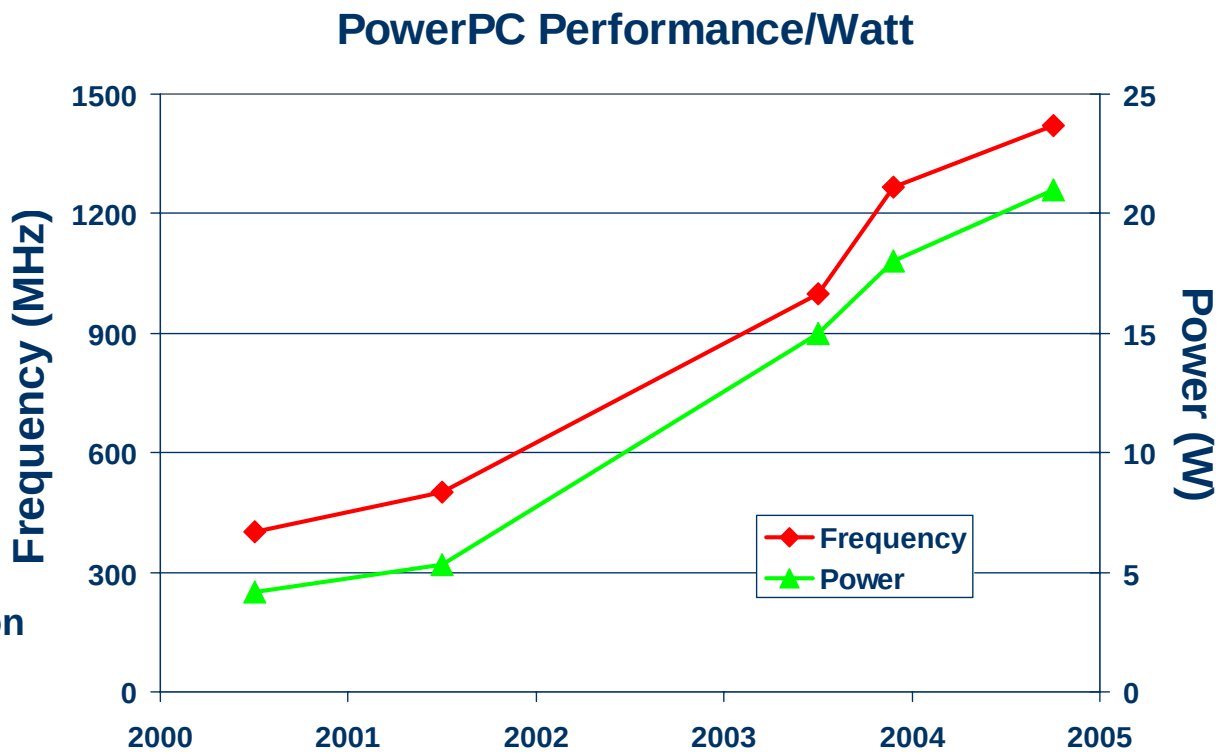
- **UAVs height is very small; tends to lead to smaller system designs than 6U arrayed on base of fuselage/wings**
- **Payload weight is small, thus weight constrained solutions are demanded**
- **UAVs tend to fly fairly high. A consequence is that without life support environments (no man) at this altitude, conduction cooled becomes mandatory.**
- **All traditional HPEC applications are represented on all the platforms.**

PowerPC Performance/Watt History

Historically, have relied on Moore's Law. Could wait and technology improvements would enable significant miniaturization. However, we observed increases in absolute performance are accompanied by increases in power, and by consequence weight and volume.

Number of transistors available is increasing, but power consumption is increasing at almost same rate. Increased infrastructure to handle power distribution and heat extraction incurs a penalty in size and weight. Alternative approaches are needed.

One approach: leverage field-programmable gate arrays (FPGAs) as programmable processors.

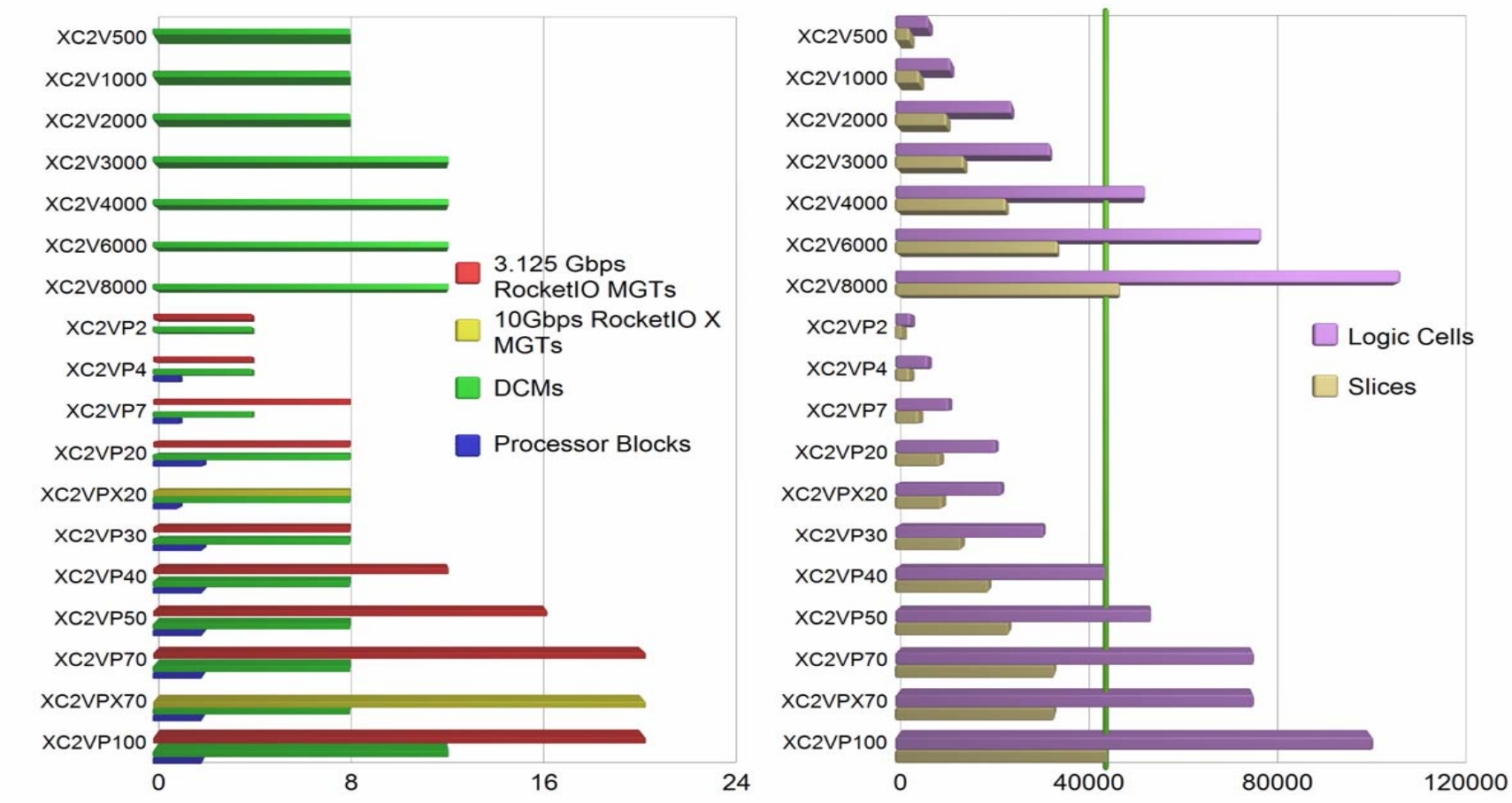


For some signal/image processing functions, FPGAs shown to provide a 10-20 fold performance boost over a PowerPC G4 processor. However, some tasks, e.g. filter weight computation, back-end processing, still perform better on a PowerPC.

In trying to maximize processing power in smallest space, trick is not only trying to find optimum balance between FPGAs and PowerPCs, but also exactly which model of each chip to choose.

FPGA Selection

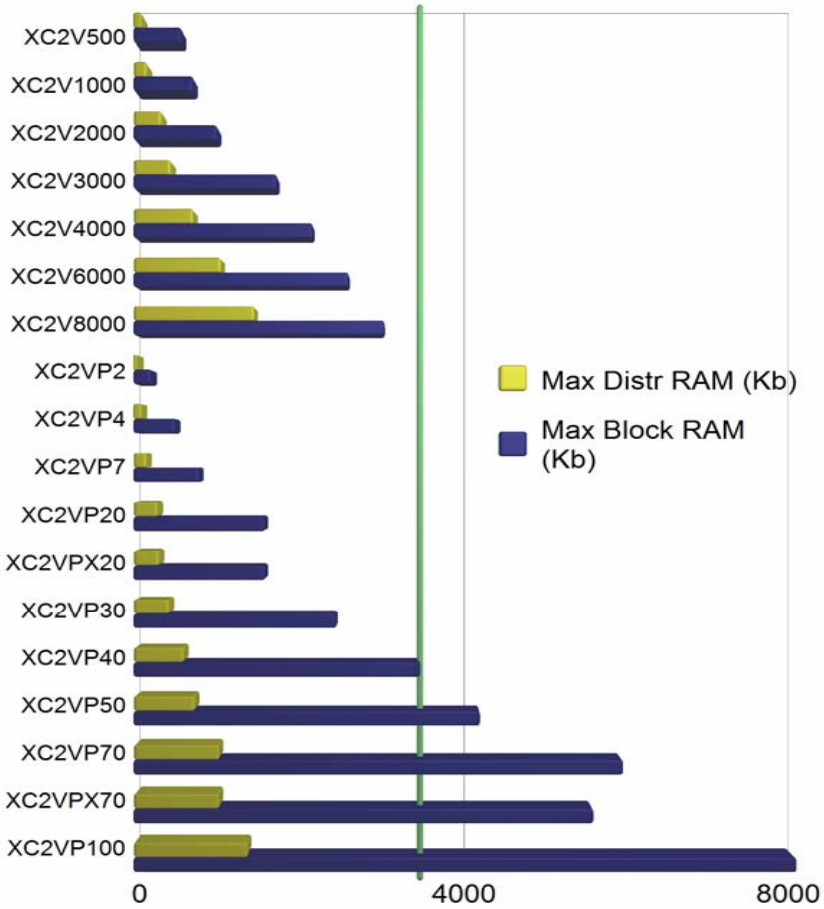
- The popular comparison….

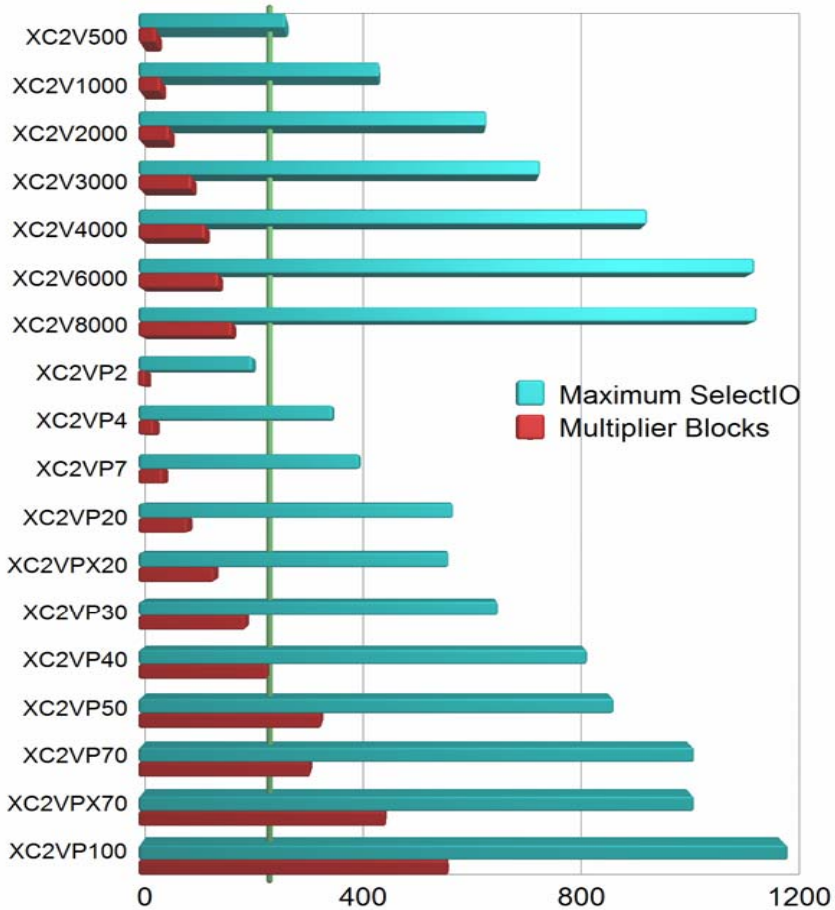


- These are the resources most often receiving attention when people look at Xilinx parts

FPGA Selection

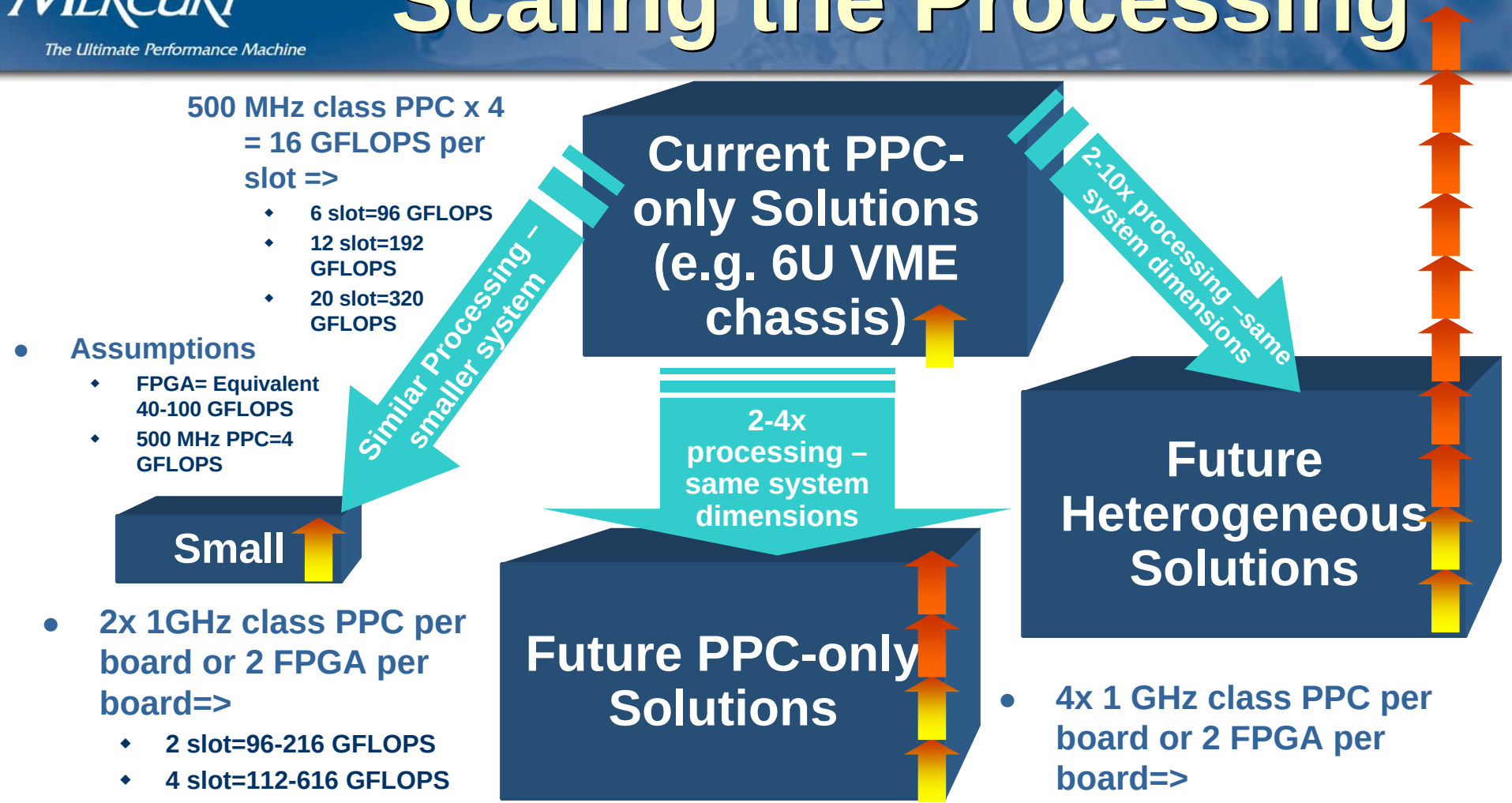
- ….But what really matters





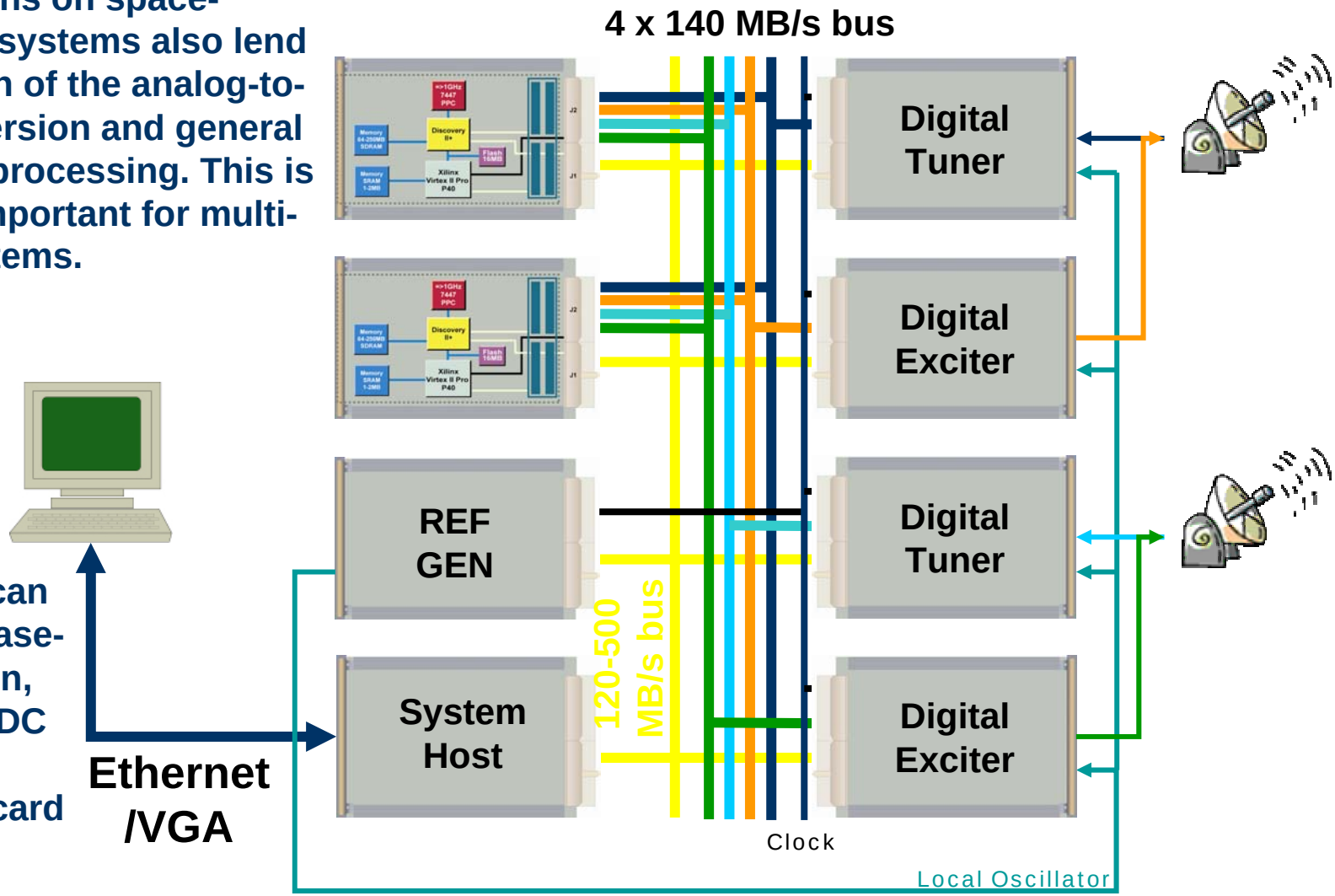
- For embedded signal/image processing applications, more critical elements tend to be number of multiplier blocks and block RAM size
- Leads to different component selection favoring Pro range

Scaling the Processing



2-Channel Software Radio

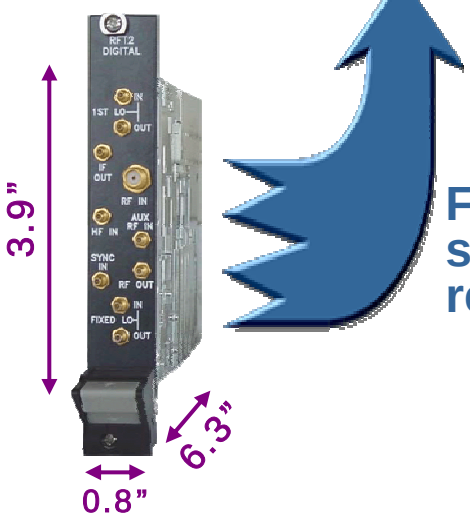
Slot limitations on space-constrained systems also lend to integration of the analog-to-digital conversion and general I/O with the processing. This is especially important for multi-channel systems.



Sensor I/O can be part of base-board design, e.g. tuner/ADC or be a mezzanine card attached to processors.

SDR Example Mapped to Enclosure

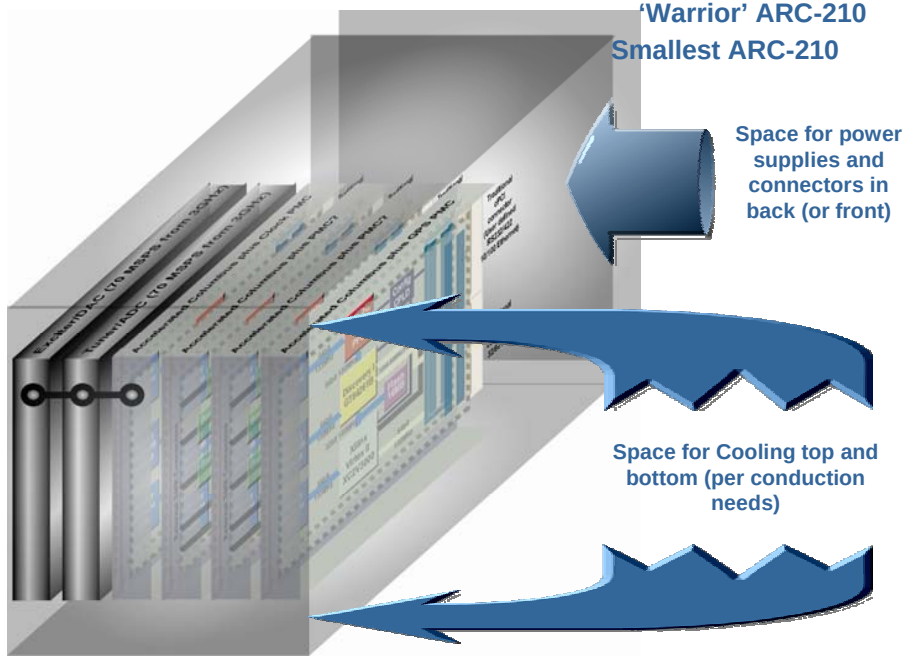
- Example ARC-210 Form



Fitting 6 x 3U cPCI slots leaves total remaining space of

- Width 1”(20%)
- Height 1.7”(>30%)
- Length 6.3”(>35%)

- MCP3 FCN + DRTi Analogue
  - dimensions to scale



- RF
  - 1 channel at 70 MSPS 14 bit input from 3GHz operating band
  - 1 channel at 70 MSPS 14 bit output to 3 GHz operating band +20dBm
- Digital = ~80-240 GFLOPs
  - 4 x 1 GHz PPCs
  - =~ 40 GFLOPs
  - 4 x Virtex II P40 FPGAS
  - =~ 40-200 GFLOP equivalent

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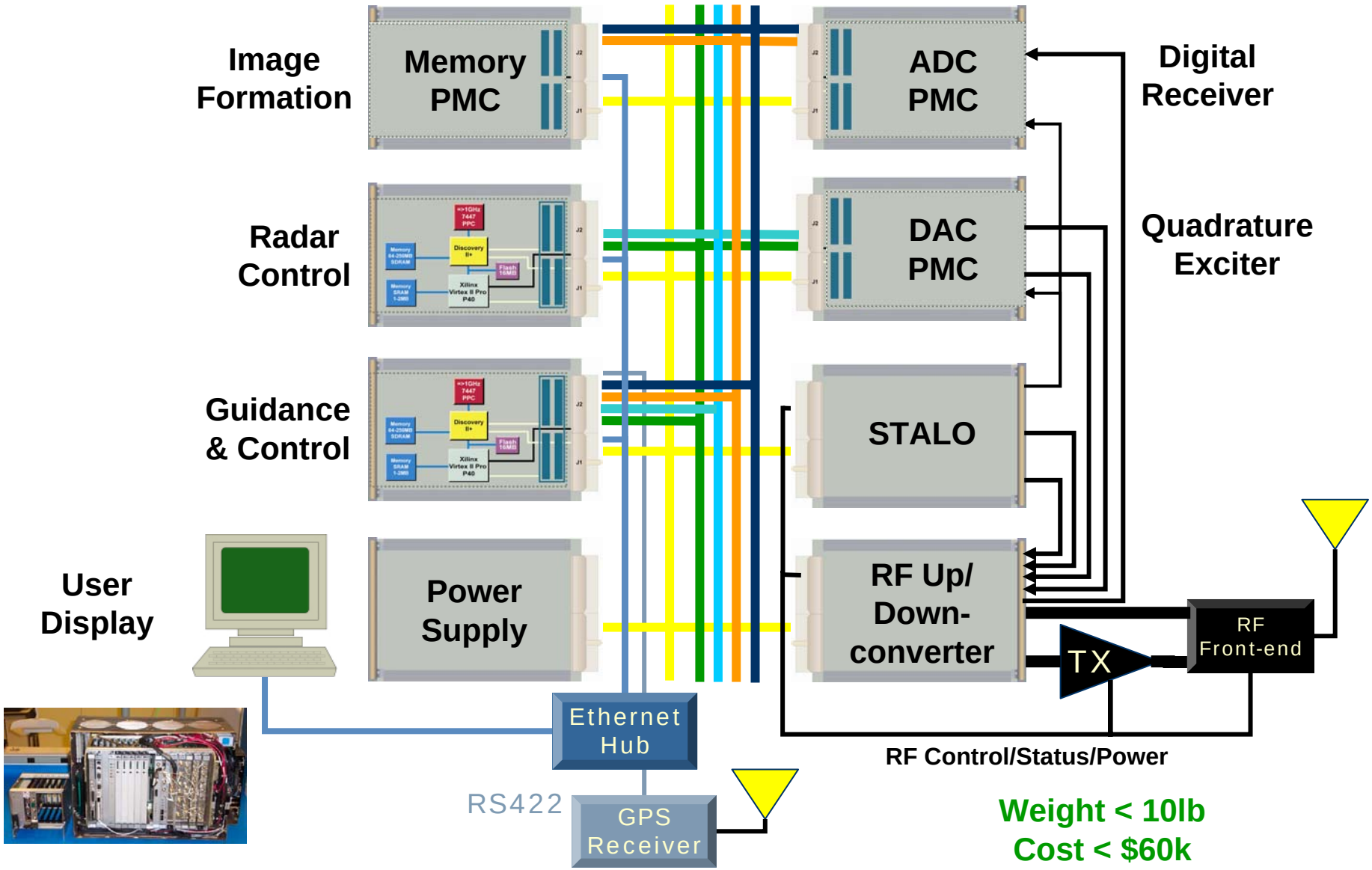
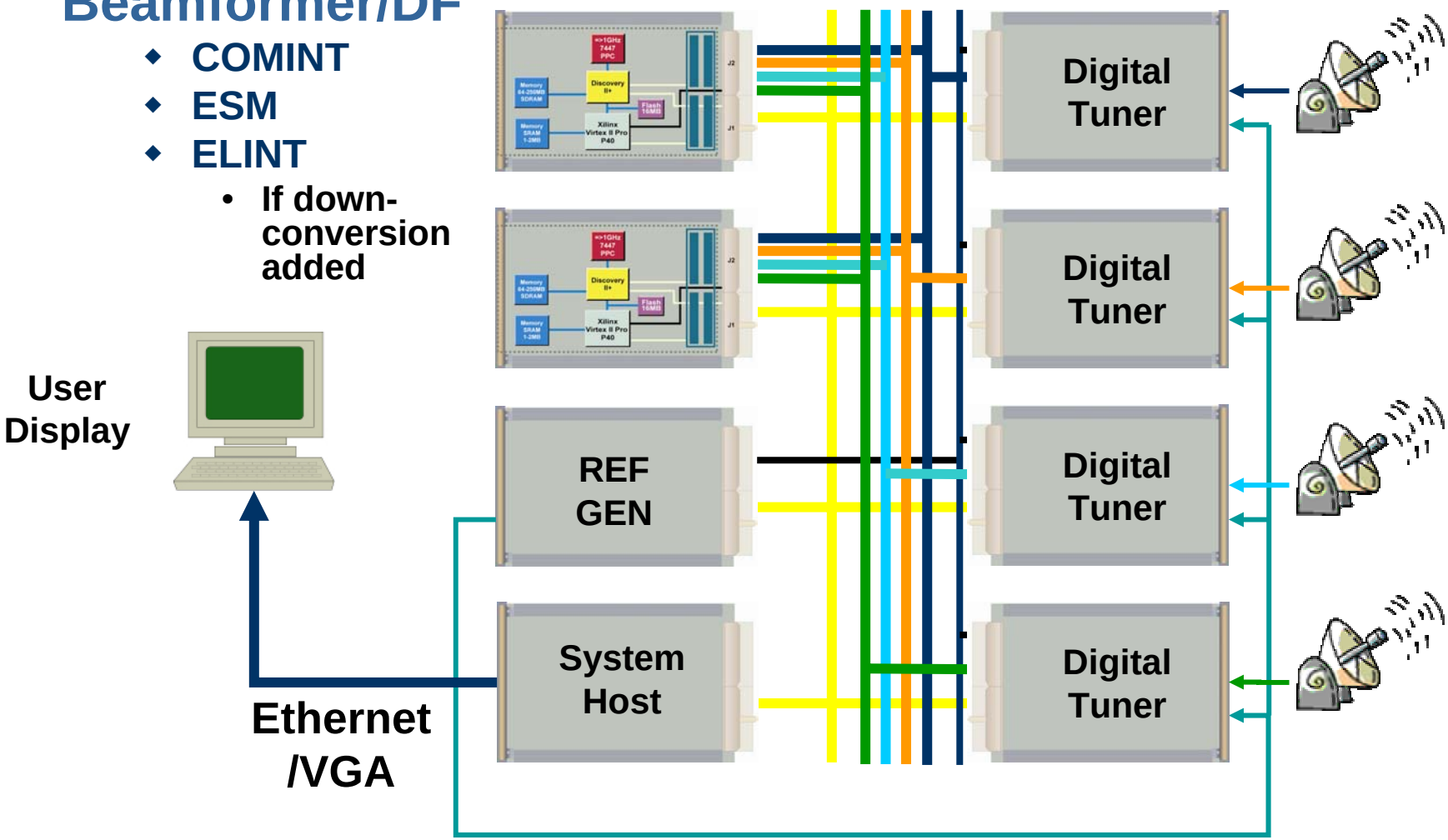
Small SAR



4-Channel Spatial Discrimination

Beamformer/DF

- COMINT
- ESM
- ELINT
  - If down-conversion added



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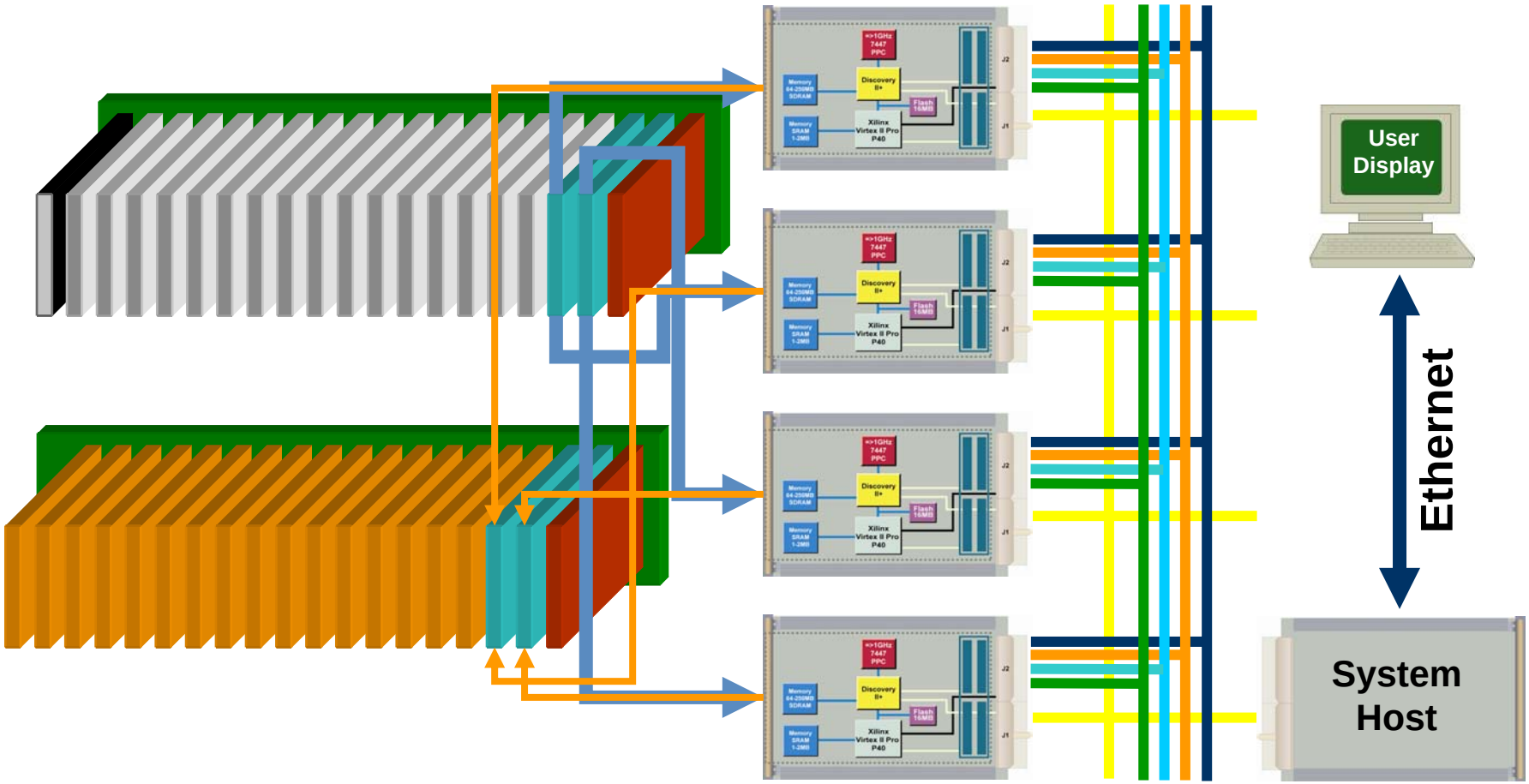
16-Channel Spatial Discrimination



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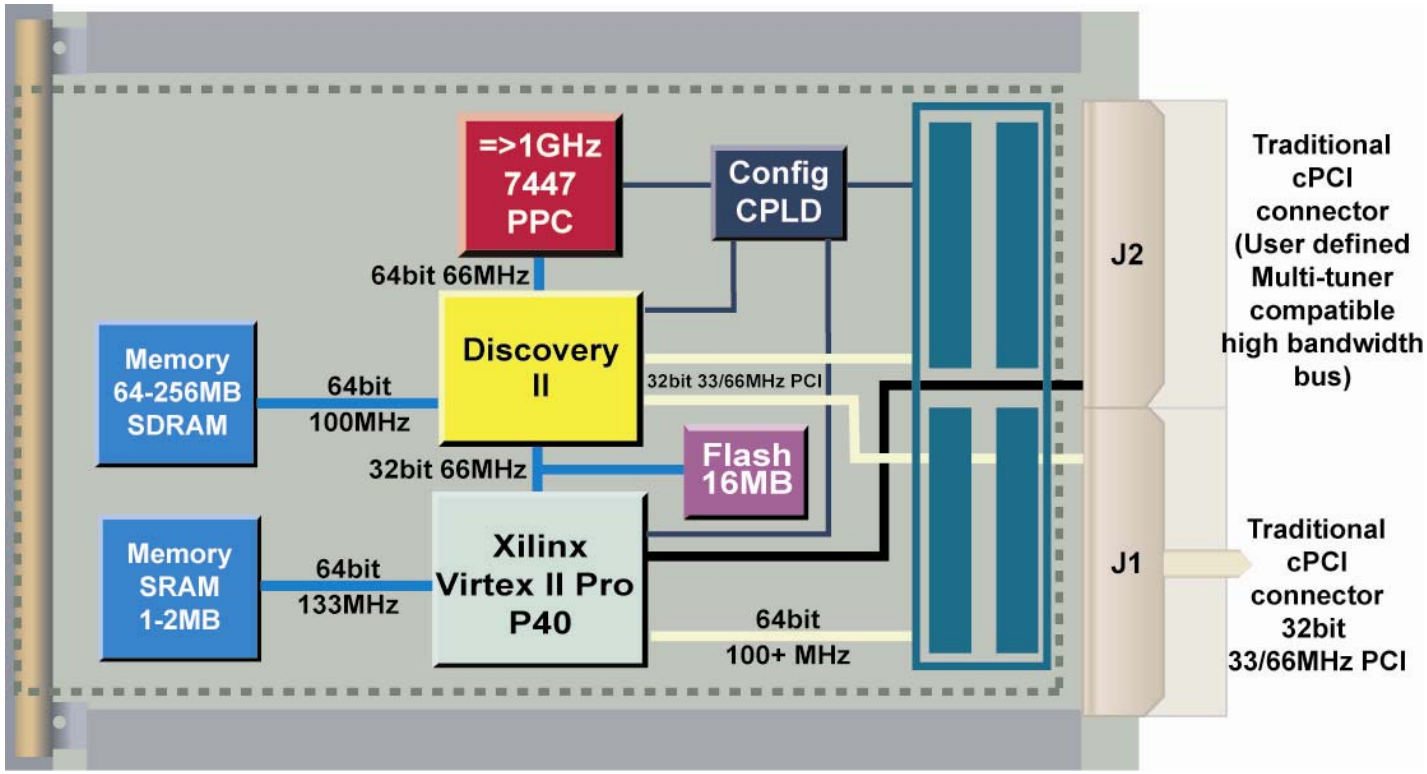
3U Design for Signal Processing



- PowerPC 7447, 1 GHz
- 250 MB/s off-board via cPCI
- MCOE 6.2.x support
- WindRiver VxWorks + Tools
- FPGA Virtex II Pro
- 4x Direct high speed ‘digital IF’ interfaces
- PMC site for digital receiver or modem etc.
- FDK 2.0.x support

MCP3 FCN: Flexible 3U Signal Processing

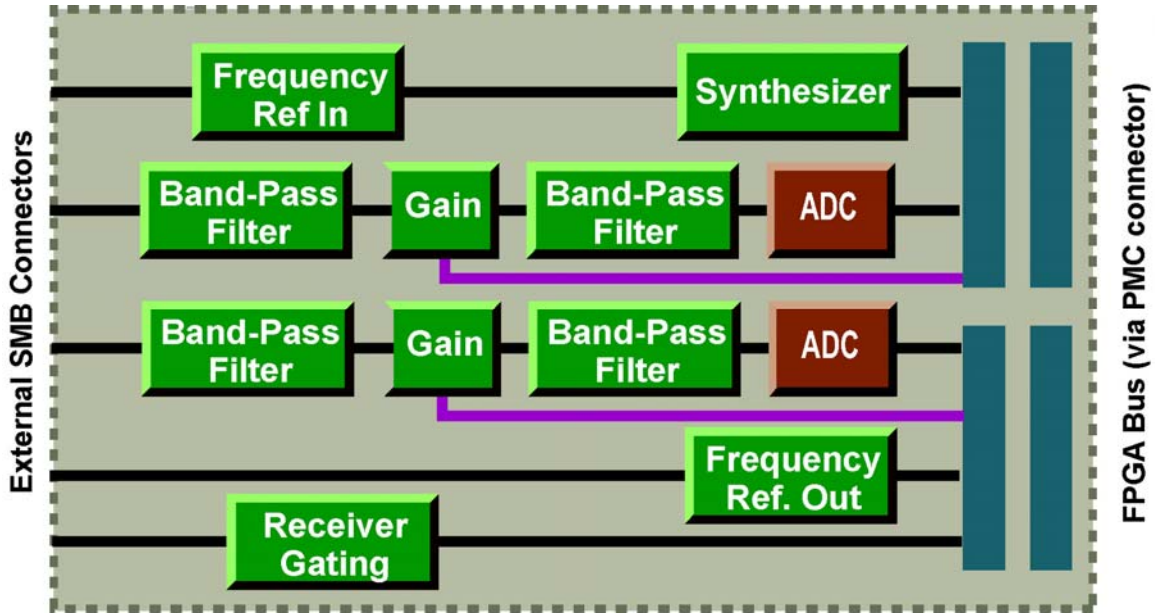
- **Combined PowerPC & FPGA**
  - Flexibility of RISC processing code
  - Density and bandwidth handling strengths of FPGAs
- **Deployable**
  - Ruggedized & conduction-cooled
- **Multiple I/Os direct to FPGA**
  - 4x high-speed bus via J2
  - Dual-channel analogue input digital receiver PMC option

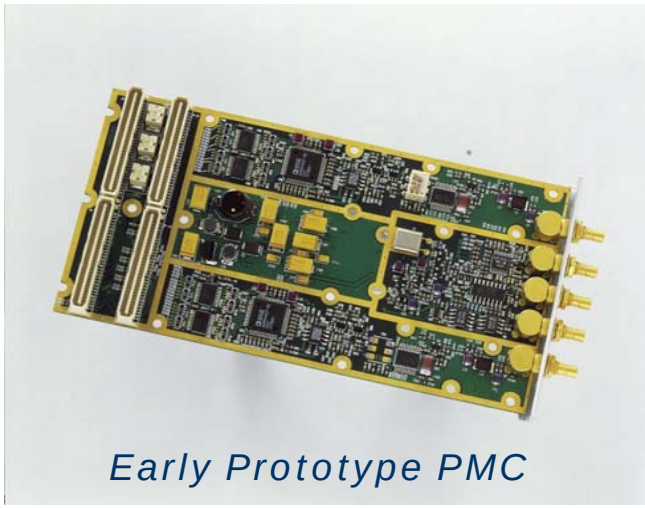
Early Prototype

Initial PMC Offering

Analog I/O receiver

- 2x 80 MSPS 14 bit ADC
- Factory configurable
  - IF up to 100 MHz





Early Prototype PMC

PMC general features

- Direct interface to FPGA
- Stepped attenuators
- RF screening
- Clocks (int./ext.)
- Power managed