Application-Specific Optical Interconnects for Embedded Multiprocessors

Neal K. Bambha
US Army Research Laboratory
Shuvra S. Bhattacharyya
University of Maryland, College Park
nbambha@eng.umd.edu, ssb@eng.umd.edu

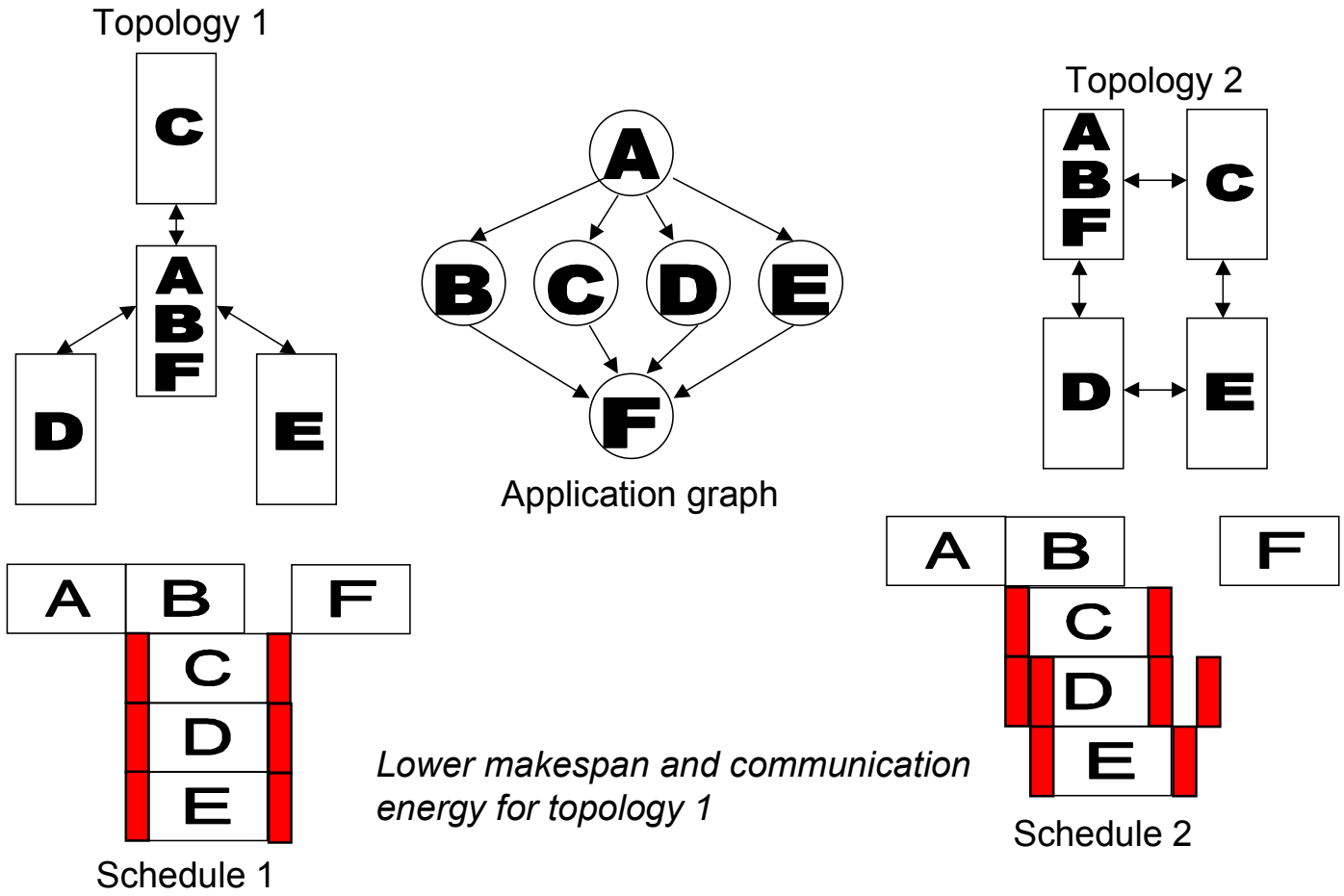
Introduction

- Develop software tools and algorithms to efficiently map digital signal and image processing (“DSP”) applications onto Systems on Chip.
  - Joint scheduling/interconnect synthesis optimization
  - Scheduling for low-hop communication on arbitrary topologies
  - Synthesize an optimal *application-specific* interconnect topology

Scheduling

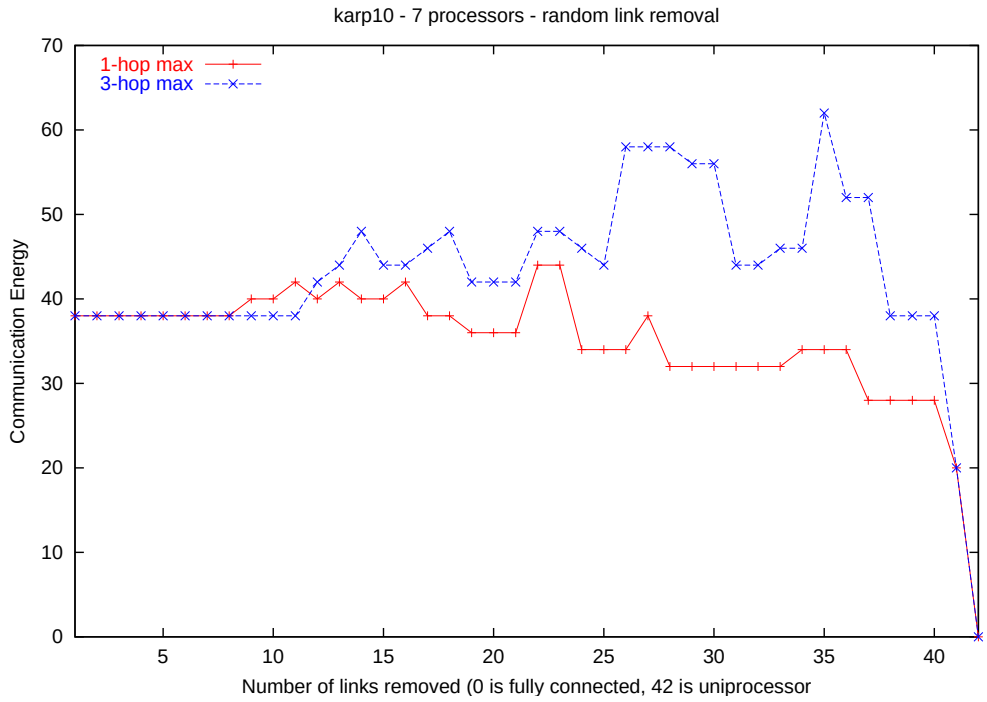
- Task graph $G(V, E)$, $\nu \in V$, $e \in E$
  - Dataflow specification
  - General point-to-point networks
- Topology graph $T(P, L)$, $p \in P$, $l \in L$
  - Link constraints
  - Processor fanout constraints
  - $l = (p_i, p_j)$ assigned weights—delay and power
  - $\mathscr{E}(G, T, n) = \sum_{e \in E} \left(\mathrm{IPC}(e) \sum_{l \in \mathrm{route}(e)} \epsilon_{\mathrm{bit}}(l) \right)$
- Communication hop limit

Effect of Topology



Lower makespan and communication energy for topology 1

Low Hop Communication Saves Energy



Compare communication energy across a range of randomly generated topologies with single-hop and 3-hop limit.

Application-Specific Interconnect Topologies

- Design constraints for optical interconnects
  - Topology—total links, maximum fanout
  - Performance—throughput, power
- Joint schedule/topology optimization
  - GA generates population of solution candidates $T(P, L)$
  - Scheduler evaluates fitness of each T
    - DLS adapted for arbitrary topologies
    - Avoids deadlock, calculates *flexibility*
    - Contructs hop-limited schedules
  - Given constraints on T, miximize performance
  - Given constraints on performance, optimize T