An Open Architecture for an Embedded Signal Processing Subsystem

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Stephen F. Shank
Principal Member
Engineering Staff

LOCKHEED MARTIN

Project Summary

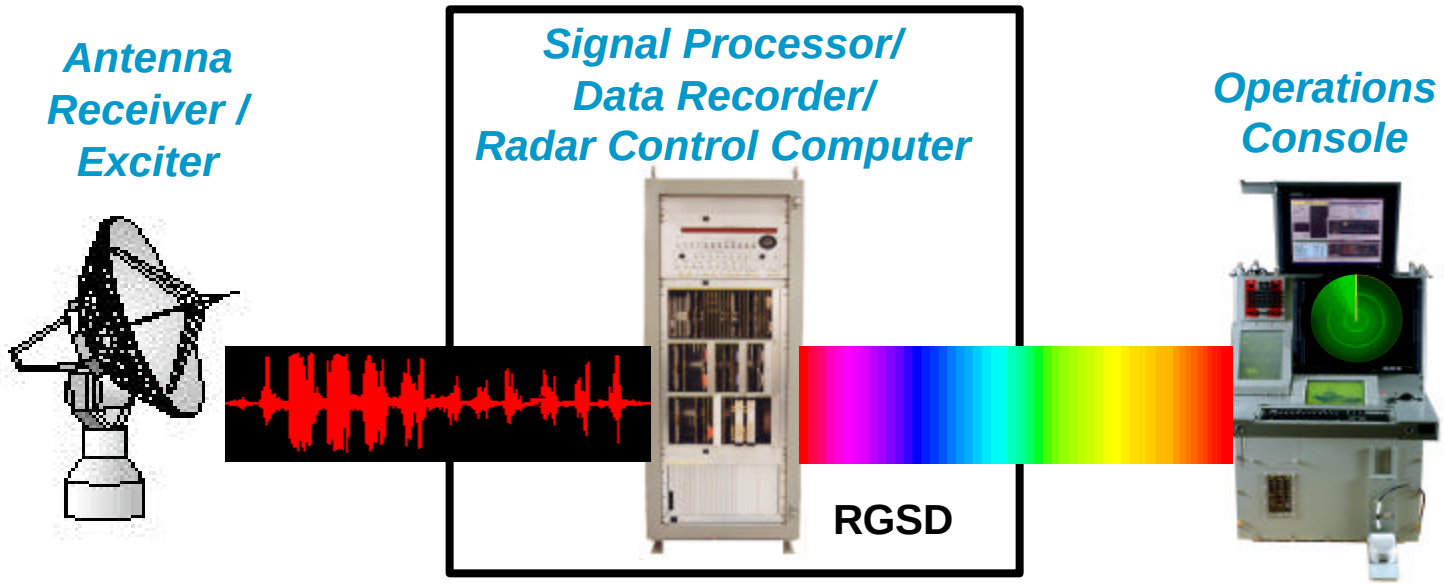
- *The Objectives:*
  - *Utilize High Performance Embedded Computing To Replace Legacy Signal Processor Equipment In Future Radar Programs*
  - *Assemble A Project Team To Define, Develop And Code The Key Functions Of The Open Architecture Digital Processor*
  - *Demonstrate A Prototype In 15 Months*
- *The Players:*
  - *Lockheed Martin – Radar Design Agent And System Integrator*
  - *INDRA –Spanish Radar Company And Software Developer*
  - *CSPI - COTS Hardware Supplier And Investment Partner*
  - *VMETRO - COTS Data Recorder*
  - *Primagraphics - COTS Display*
- *Lockheed Martin Tasks:*
  - *Develop The Hardware / Software Architecture*
  - *Define Target Radar Characteristics And Provi... Matlab Models,*
  - *Conduct Integration And Test Activities*
- *INDRA Tasks:*
  - *Design, Develop, Code, And Test Key Functions Of The COTS DSP*
  - *Support Integration & Test*
- *CSPI Tasks:*
  - *Provide Training To INDRA*
  - *Provide Hardware And Software Development Environment*
  - *Develop Radar Interface Boards*
  - *Provide Development Support*
- *VMETRO:*

... Display Equipment

International Development Team Assembled

Project Plan:

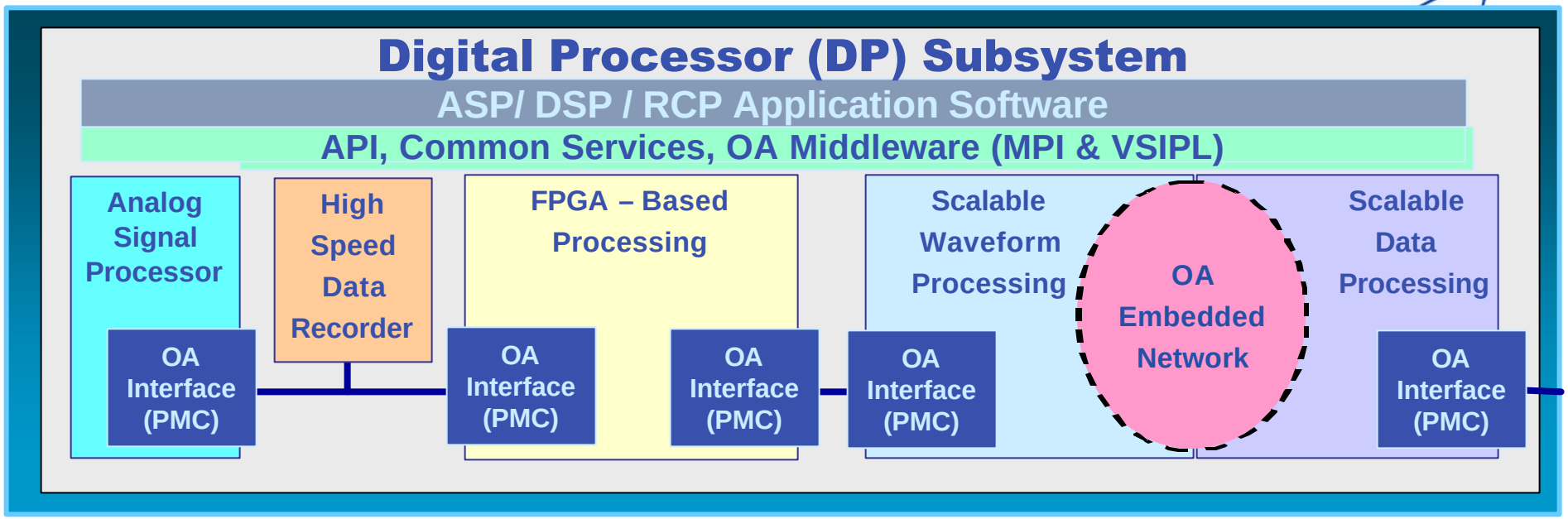
Reconfigurable Generic Search Radar Digital Signal Processor (RGSD)



- ***Define radar characteristics, specifications, Matlab Models and system interfaces***
- ***Develop a flexible hardware / software architecture***
  - *Software is reusable and scalable*
  - *Hardware is scalable and refreshable*
- ***Conduct Integration and Test activities in radar test bed***

Demonstrate RGSD in a Legacy Radar in 15 months

Open Architecture Digital Processor

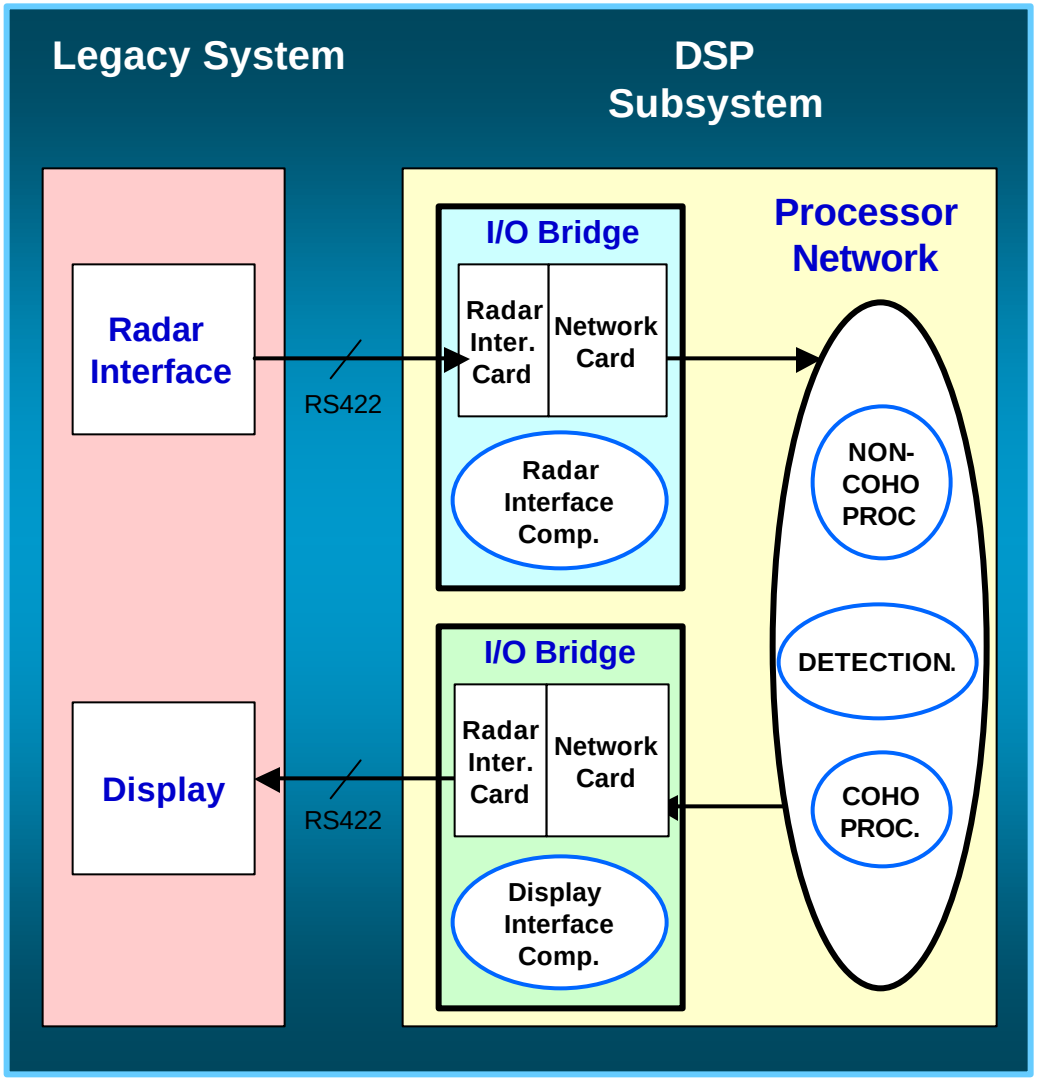


- *Software - Object-Oriented, C/C++*
- *Requirements Management – Telelogic DOORS*
- *OO Modeling – Rational Suite (Rose)*
- *Configuration Management – Rational ClearCase*
- *Integration & Test – VxWorks Tornado 2*

- *Standard API, OA Middleware*
  - *Open Message Passing Software*
    - *MPI & TCP/IP*
  - *Standard Signal Processing Libraries*
    - *VSIPL*
  - *Support for Open Architecture Standards*
    - *VME 64, Fibre Extreme, PCI/PMC capable, Myrinet*

Independent, Scalable,Reusable Software

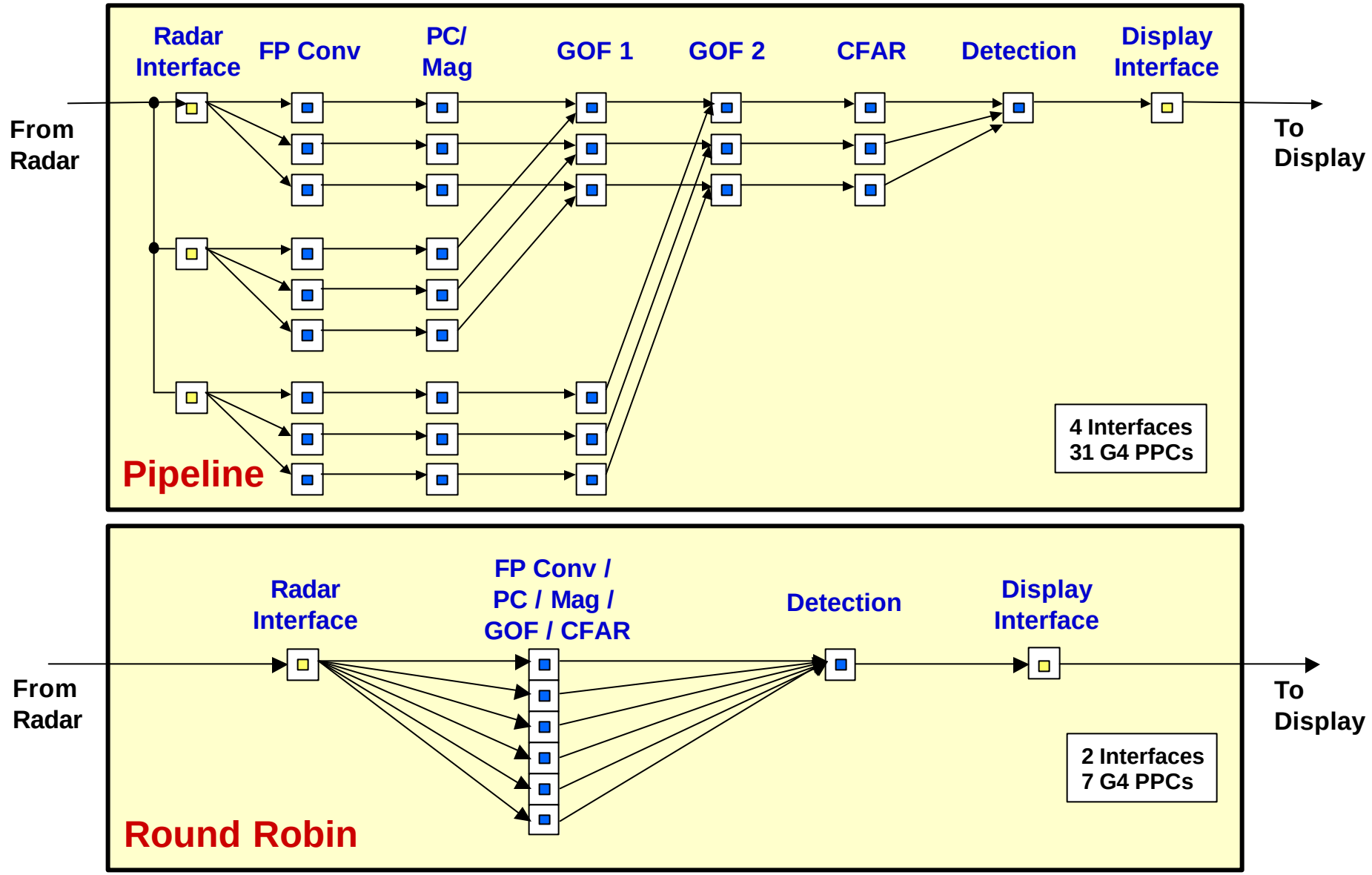
RGSD Development Methodology



- *Determine Processing Requirements for Waveform Suite*
- *Partition Processing Requirements into 5 Functional Groups*
  - *Radar Interface Component*
  - *Display Interface Component*
  - *Coherent Waveform Processing*
  - *Non-Coho Waveform Processing*
  - *Detection*
- *Map Algorithm Functionality to Processor Configuration*
- *Identify Potential Risk Areas*
  - *Processing Intensive (e.g. Match Filtering)*
  - *I/O Intensive*
- *Design Software using*
  - *High Level Language (C/C++)*
  - *Common Application Programmer's Interfaces (API) such as MPI/VSIPL for scalability and portability*
- *Validate Software against MatLab Hardware Model*

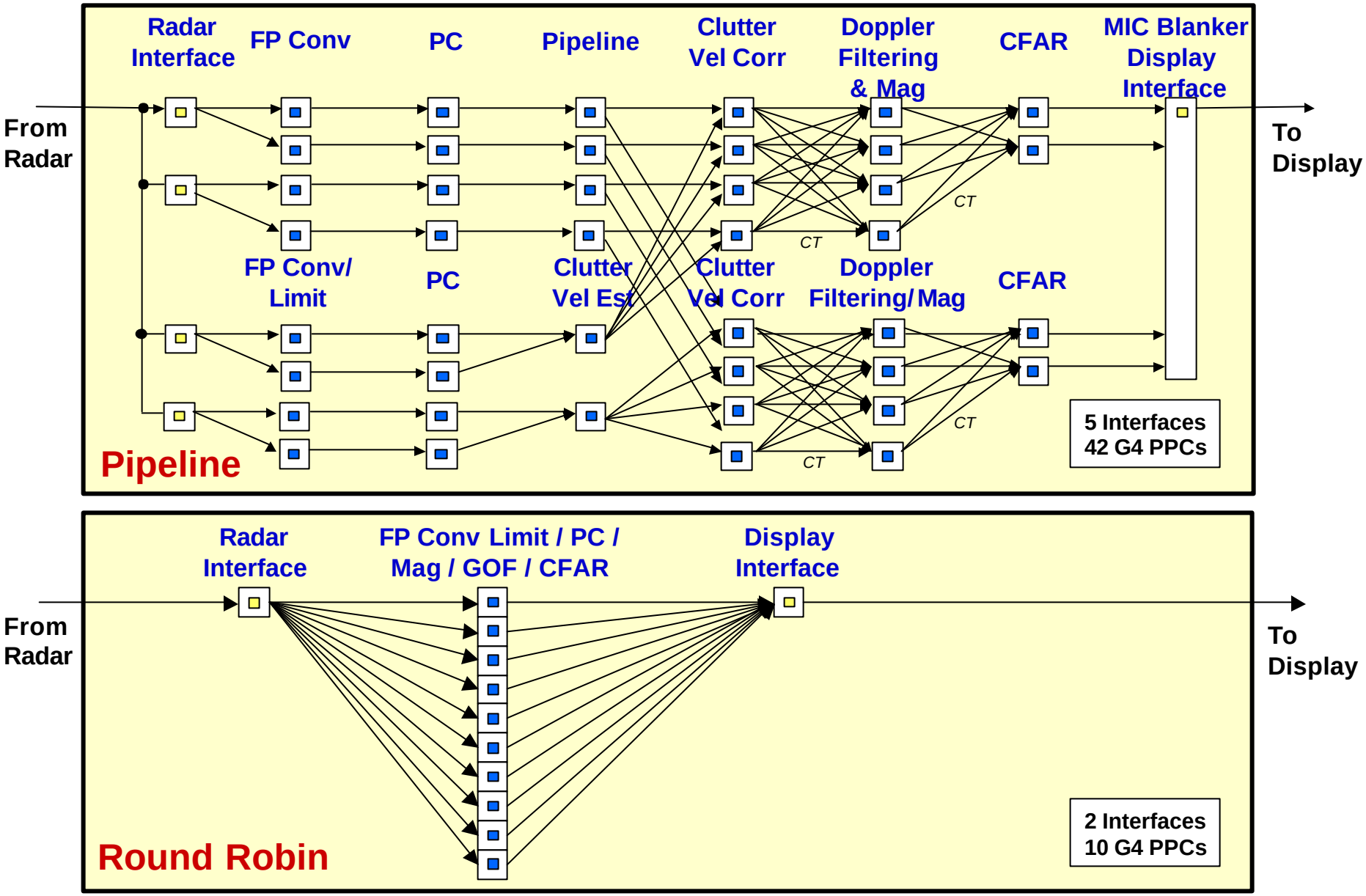
Non Coherent Processing Architecture

-Two Options:

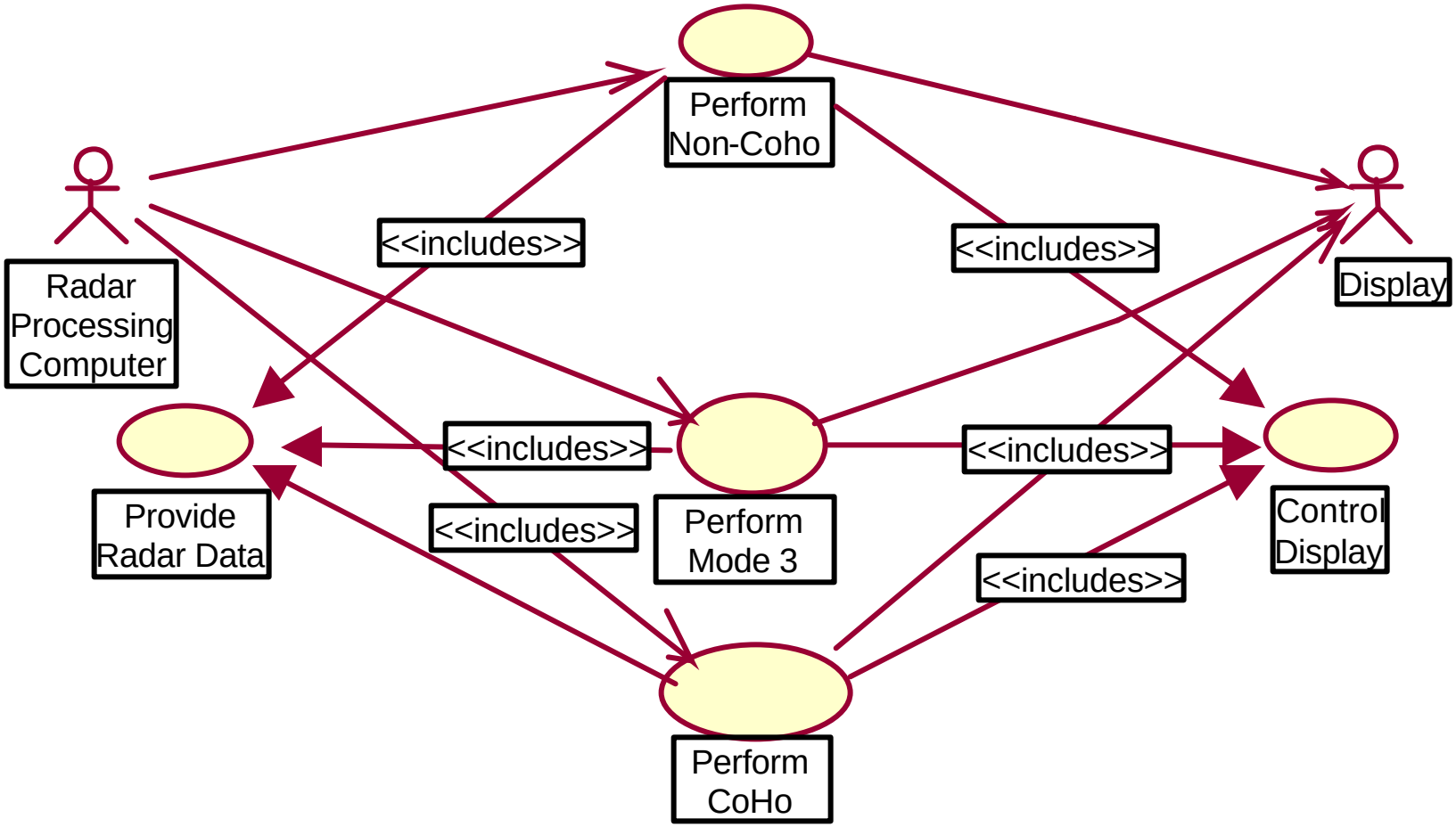


Coherent Processing Architecture

-Two Options:



Top Level RGSD Use Case Diagram



Visual Modeling maximizes the team's development productivity

Architecture Comparison

Cost Drivers

Latency (µs)

Waveform	Estimate Pipeline	Estimate Round Robin	Actual Round Robin
Non-Coho 1	7,140	5,540	2,270
Non-Coho 2	3,570	3,710	1,970
Non-Coho 3	3,570	1,920	900
Coho 1	14,480	19,760	15,620
Coho 2	15,360	22,130	18,210

Number of PPCs (G4)

Waveform	Estimate Pipeline	Estimate Round Robin	Actual Round Robin
Non-Coho 1	31	7	3
Non-Coho 2	25	5	5
Non-Coho 3	11	3	2
Coho 1	42	9	9
Coho 2	35	10	10

Processing (%)

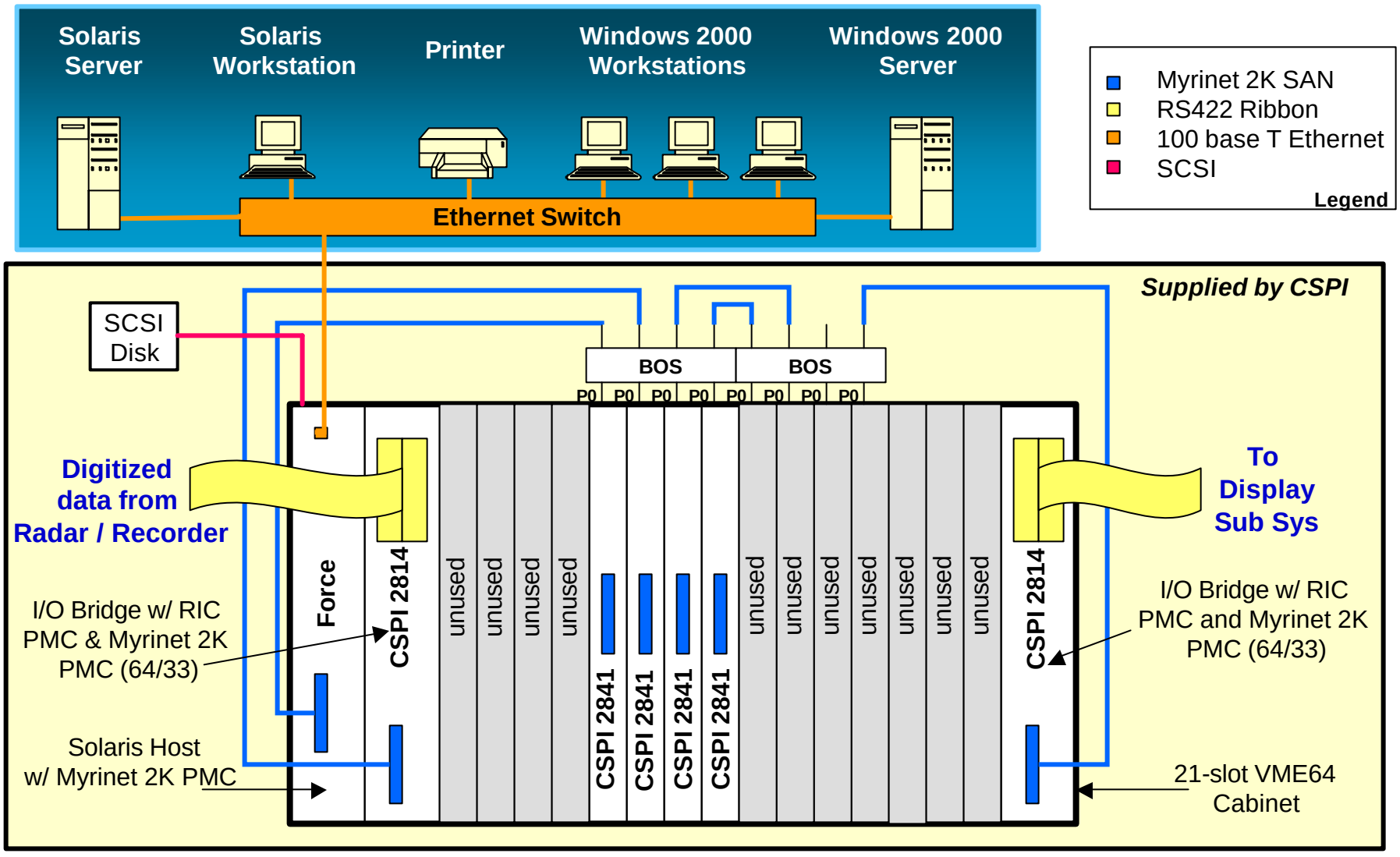
Waveform	Estimate Pipeline	Estimate Round Robin	Actual Round Robin
Non-Coho 1	49	96	89
Non-Coho 2	62	94	87
Non-Coho 3	50	88	71
Coho 1	58	91	89
Coho 2	55	90	87

I/O (%)

Waveform	Estimate Pipeline	Estimate Round Robin	Actual Round Robin
Non-Coho 1	51	4	11
Non-Coho 2	38	6	13
Non-Coho 3	50	12	29
Coho 1	42	9	11
Coho 2	45	10	13

Round Robin Meets Requirements with Fewer Processors

RGSD Development System Configuration



Open Architecture with Scalable Performance

Dual Radar and Display Interface

- *Provides in a PMC Form Factor*
  - *RS-422 Interface to Radar Processor and Display console*
  - *User programmable CPLD*
  - *High performance (64/66) PCI controller providing a high bandwidth/low latency connection between the CPLD and the PMC connectors*

Radar Interface Personality

- ***Buffers and packetizes I / Q data***
- ***DMA's packets to host memory for access by MPI***
- ***Supports Test Data Injection***
- ***Round-Robin queuing of radar data to destination software component based on waveform***

Display Interface Personality

- ***DMAs data from host memory***
- ***Sorts packets***
- ***Buffers packet in preparation for display***
- ***Restores time characteristics for proper display***
- ***Generates output signals (data and synchronization) to display console***

Hi-Performance Programmable Interface

Project Summary

- ***RGSD Prototype was successfully integrated at Lockheed Martin***
  - *System Integration and Test completed in less than three weeks*
    - *Successful use of Matlab model of legacy hardware substantially reduced I&T effort*
- ***RGSD will be leveraged for future radar programs***
  - *Addresses production cost and Diminishing Material Supply (DMS) issues of current systems by replacing legacy equipment with COTS*
  - *Software based OA design provides the ability to enhance or modify system operation without the need for major redesigns*
- ***Project validated benefits of High Performance Embedded Computing***
  - ***Reduces Cost for:***
    - *Development effort*
    - *Acquisition / Life Cycle Cost*
  - ***Provides:***
    - *Scalable and Reusable Signal Processing Software applicable to a wide variety of radar applications*

Cost Effective use of OA Standards for Real Time Radar Applications