ESSEX

Hybrid Optical/Digital Processor for Radar Imaging

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Keith Frampton
Essex Corporation
9150 Guilford Road
Columbia, MD 21046
301-953-7875
Frampton@essexcorp.com

Pat Stover
Annapolis Micro Systems
190 Admiral Cochrane Dr. Suite 130
Annapolis, MD 21401
410-841-2514
Patrick.stover@annapmicro.com

Problem Statement and Solution

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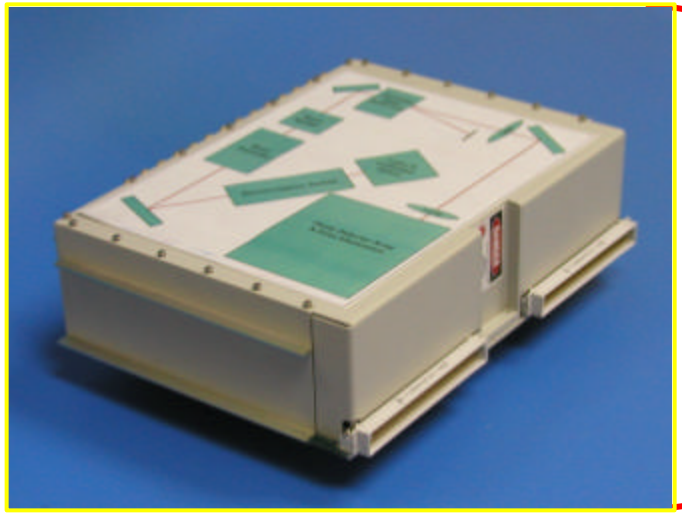
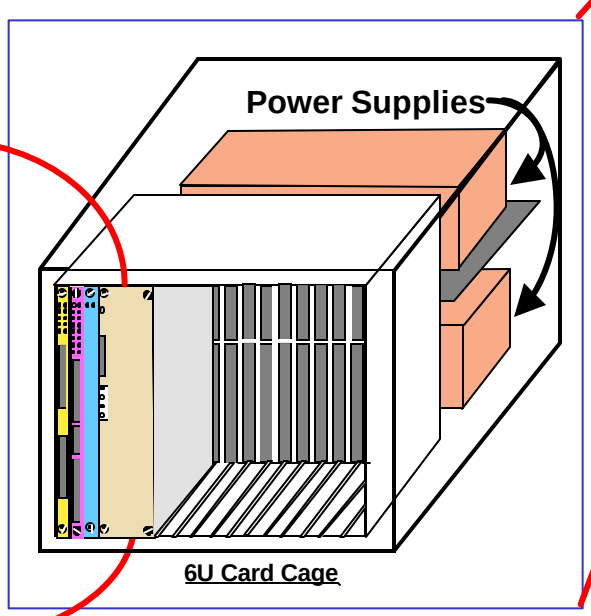
- **Problem:**
  - **Projected BMD threat environment will have clutter and EMI**
  - **LFM waveforms have limitations with these threats**
  - **Desired advanced waveforms (chaotic, PRN*, …) are very processing intensive**

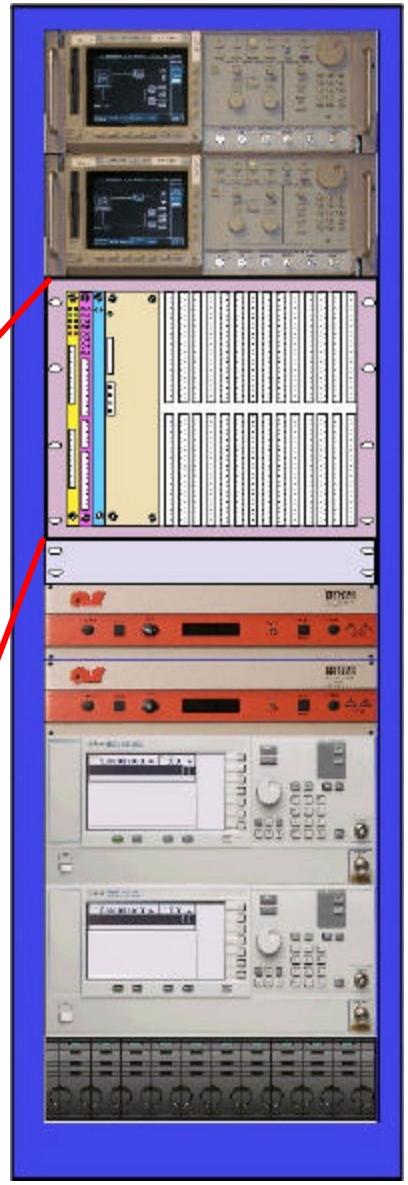
- **Solution:**
  - **The advanced optical processor (AOP) generates range-Doppler images from advanced arbitrary waveforms**
  - **AOP architecture incorporates:**
    - **Embedded optical signal processing**
    - **Embedded digital signal processing in FPGAs**

Program Objectives

- **Modernize the architecture, scaling to:**
  - **1 GHz**
  - **Real-time operation**
  - **Full complex, single pass**
  - **Store images in real-time to disk**
- **Compact rack stackable configuration**



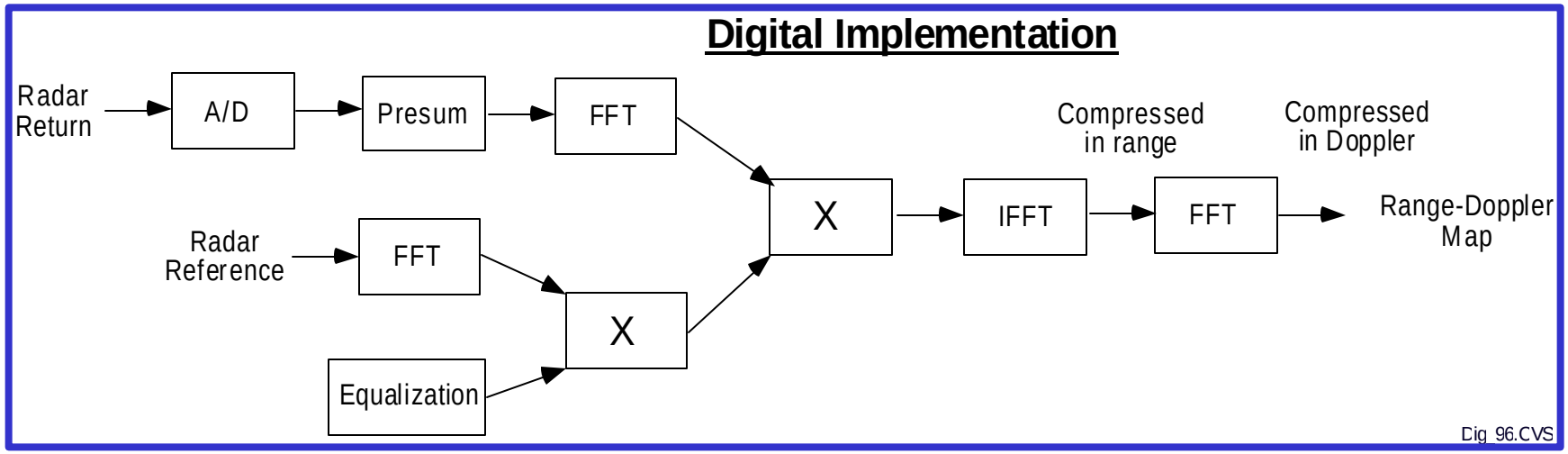


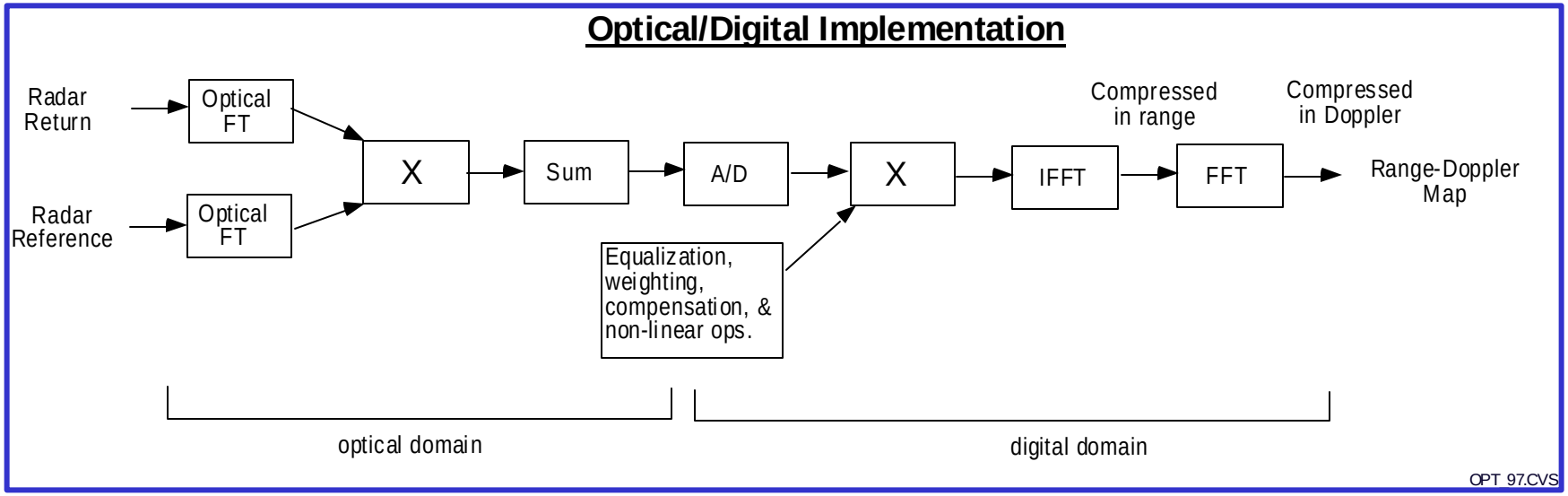


AOP 2 Performance Characteristics

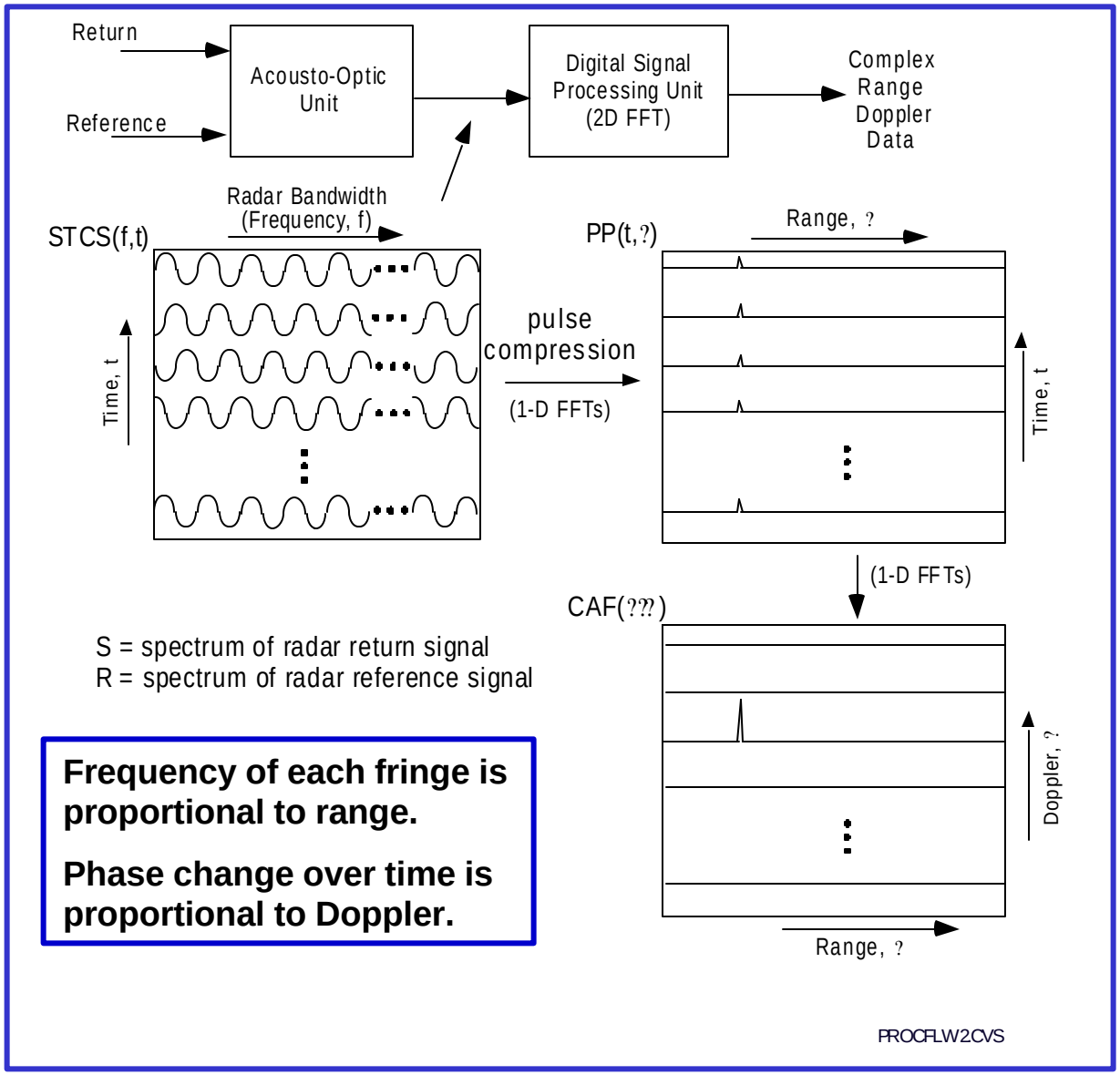
Pulse Width	10 ? sec to 50 msec
Pulse Repetition Interval (PRI) Pulse Repetition Frequency (PRF)	100 usec minimum 10 kHz maximum
Center Frequency	Tunable 5 GHz to 7 GHz (TBR)
Bandwidth (-3dB)	1 GHz
Stable Reference Frequency	10 MHz
Post-Compression Dynamic Range (peak to RMS noise)	66 dB
Spur Free Dynamic Range	85 dB for 128 coherently integrated pulses
Range Resolution	0.15 meters
SNR Loss vs. Range center	6 dB maximum @ +/- 76.7 meters relative to image center
Range Bins	1024 bins (+/- 512 about image center)
Range Extent	153 meters (+/-76.7 m about image center)
Range Sidelobes (Hamming weighting)	-34 dB
Frequency Response	3 dB uncorrected; 1 dB corrected
RCS Repeatability	+/- 0.1 dB
Phase Deviation from Linear in CPS	+/- 5 degrees

Algorithm Functionality is Similar





Process Flow

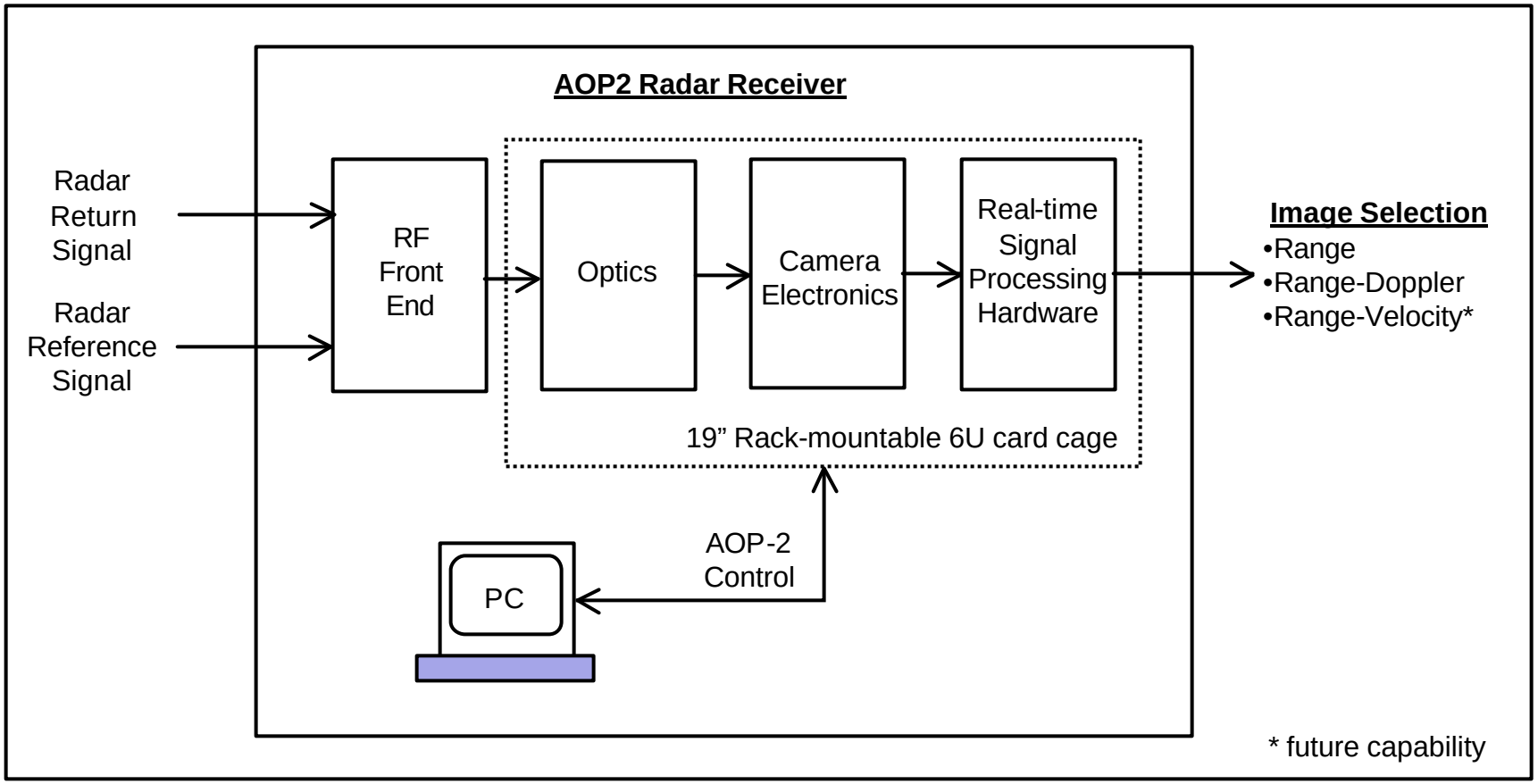


Cross power spectra vs. time

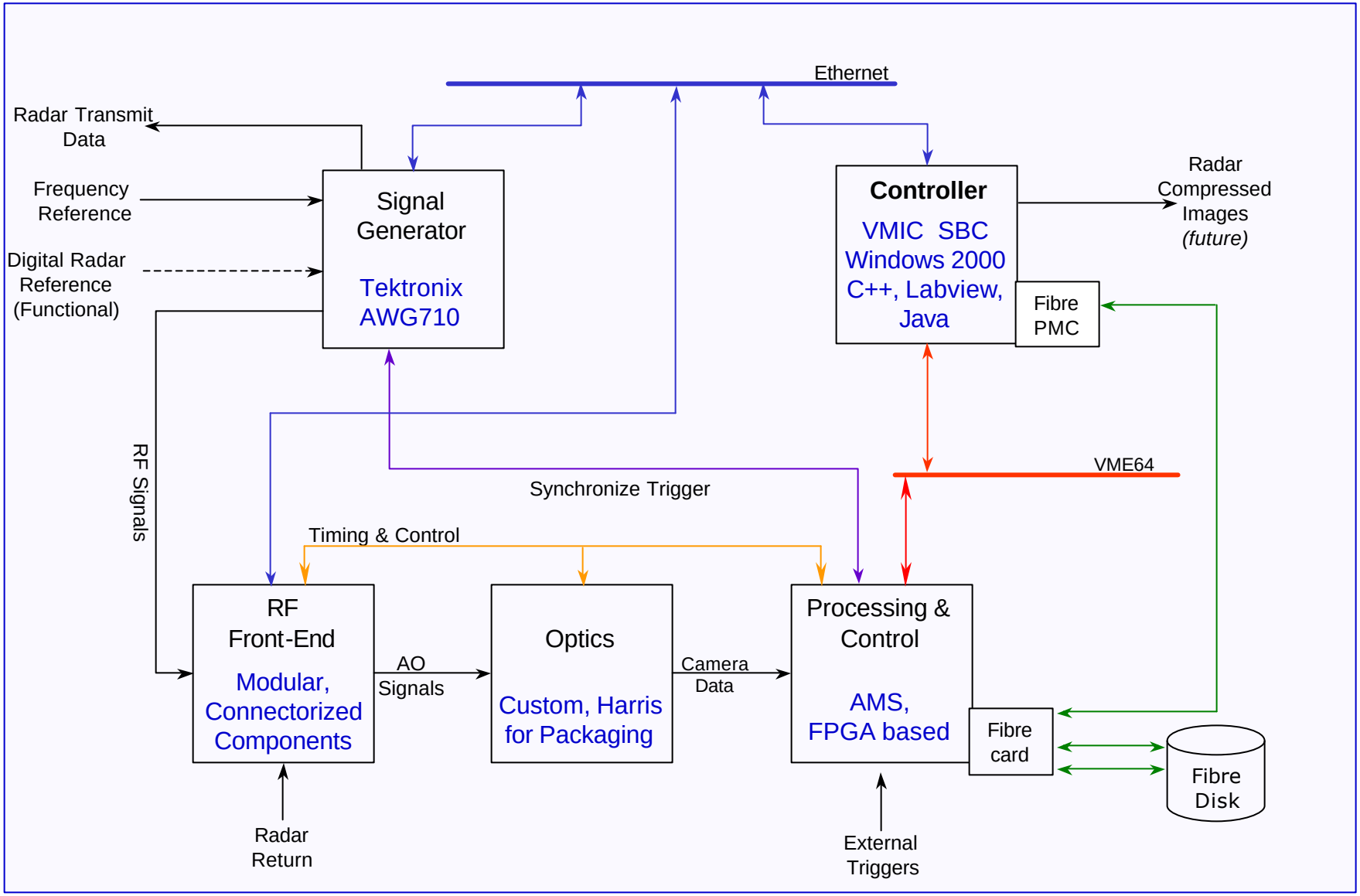
Correlator compresses pulse in range

FFT compresses pulses in Doppler

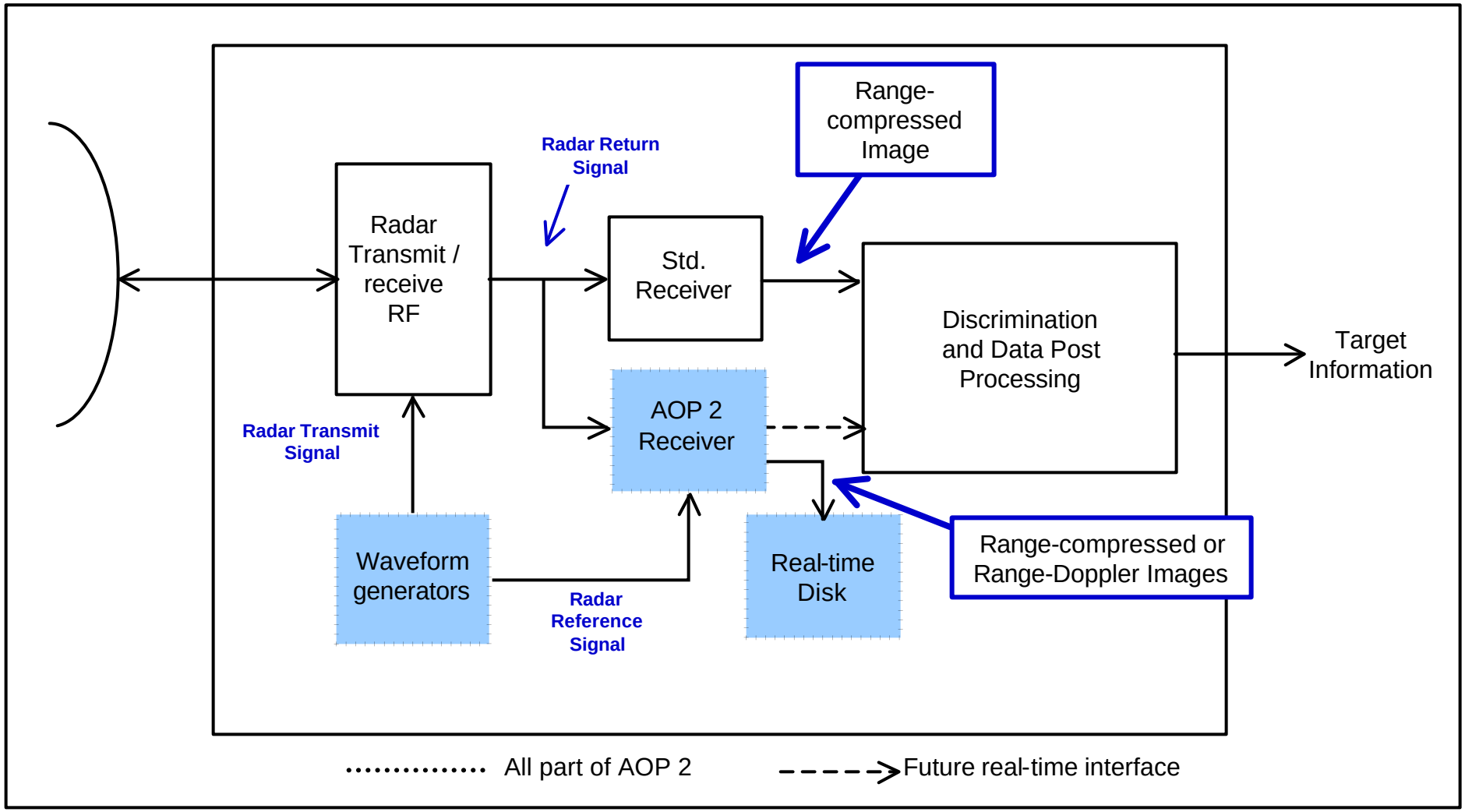
AOP2 Functional Configuration



AOP 2 Top Level System Diagram

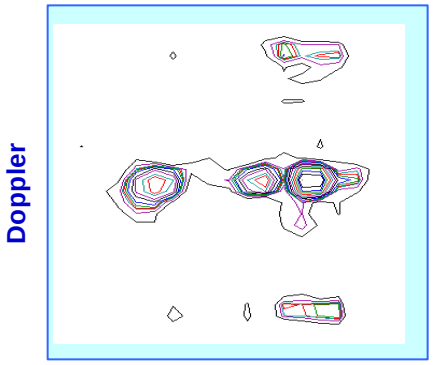


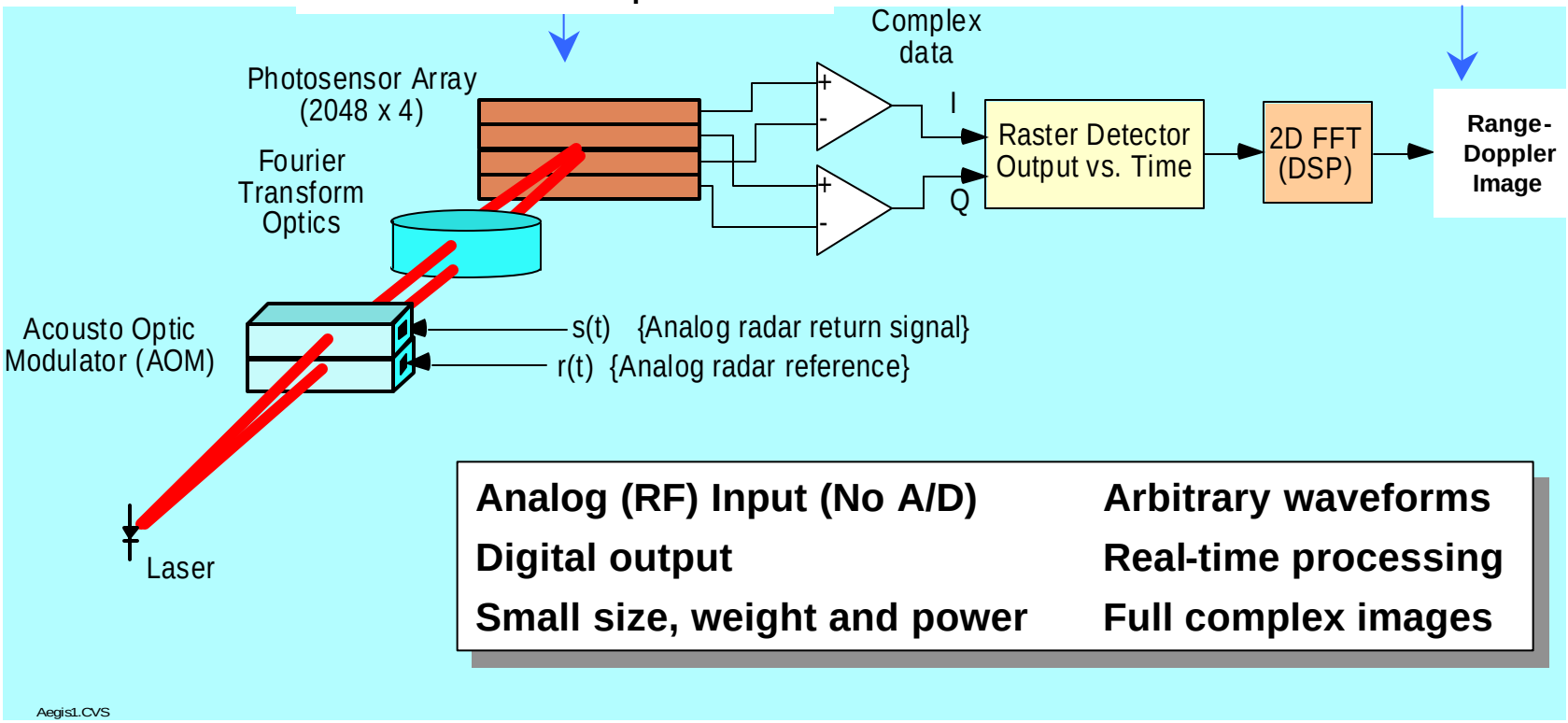
Radar Configuration with AOP2



Full Complex, Wideband Architecture

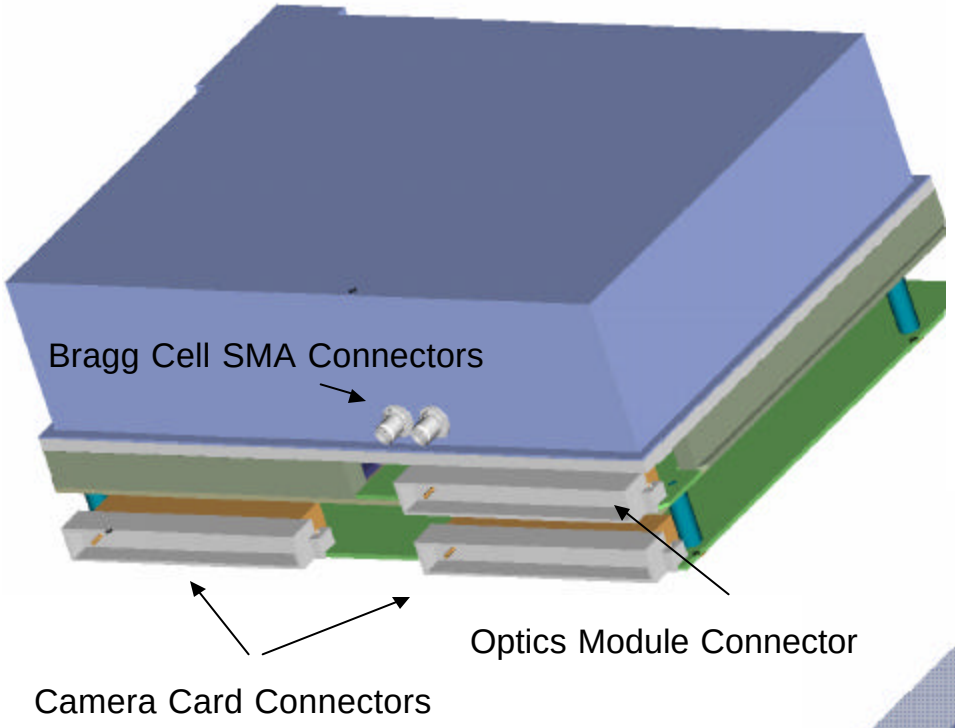
AOP2 Configuration



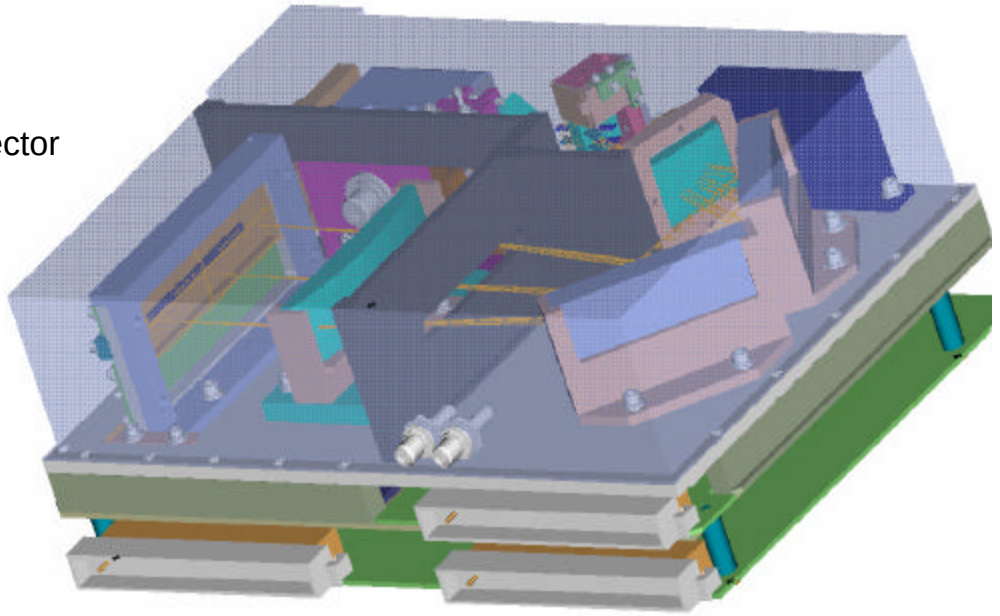


Analog (RF) Input (No A/D)	**Arbitrary waveforms**
Digital output	**Real-time processing**
Small size, weight and power	**Full complex images**

Optics Module Mated With Camera Module

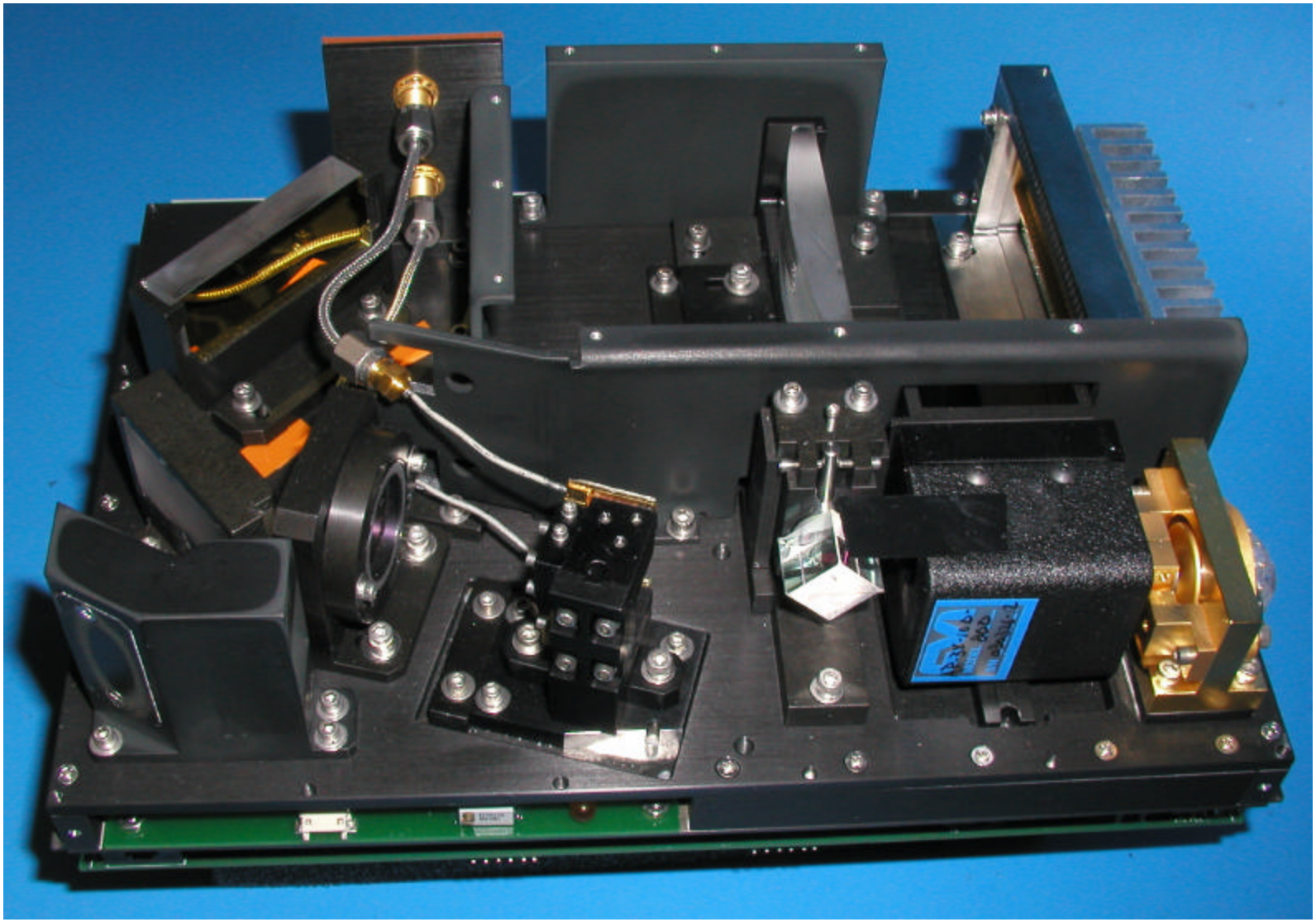


Optics Module
Optics Processing Module
Camera Card



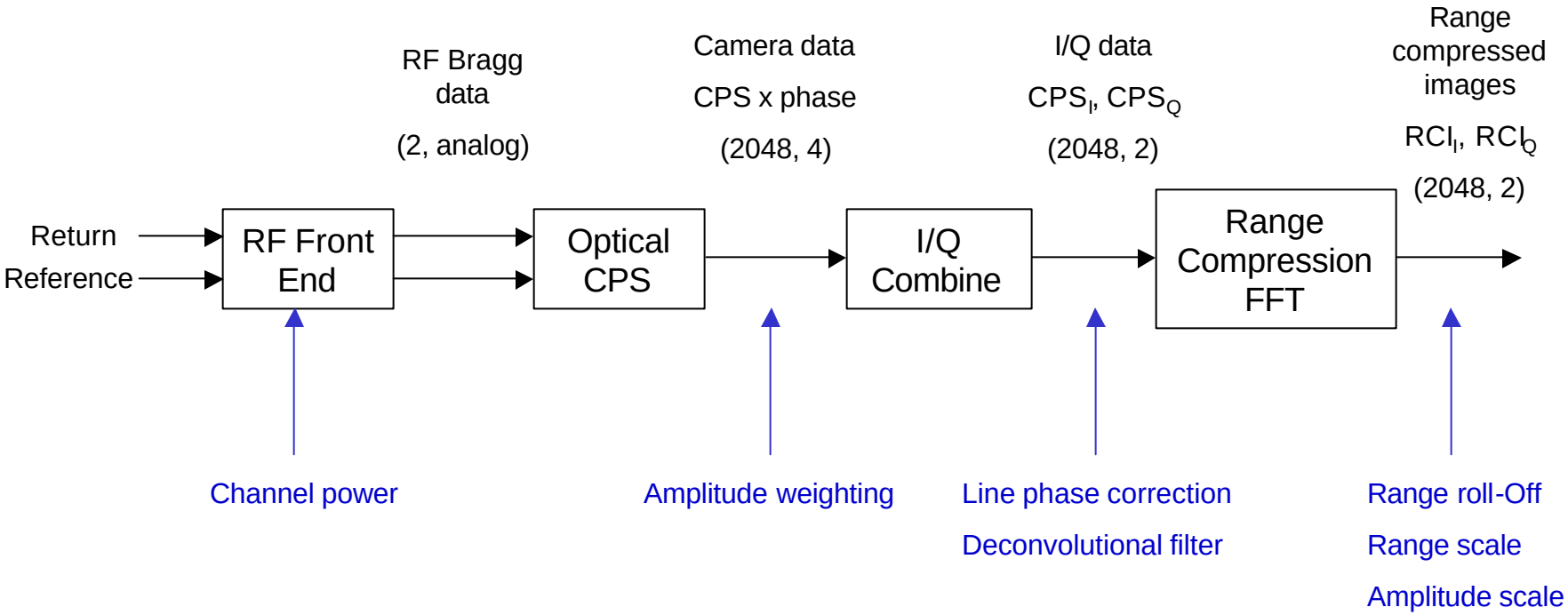
6U VME form factor

AOP2 Optics Module



System Calibrations and Corrections

- **Calibrations and corrections are required at various points in the processing chain**
  - **Correct radar and processor response**
  - **Obtain optimum performance**



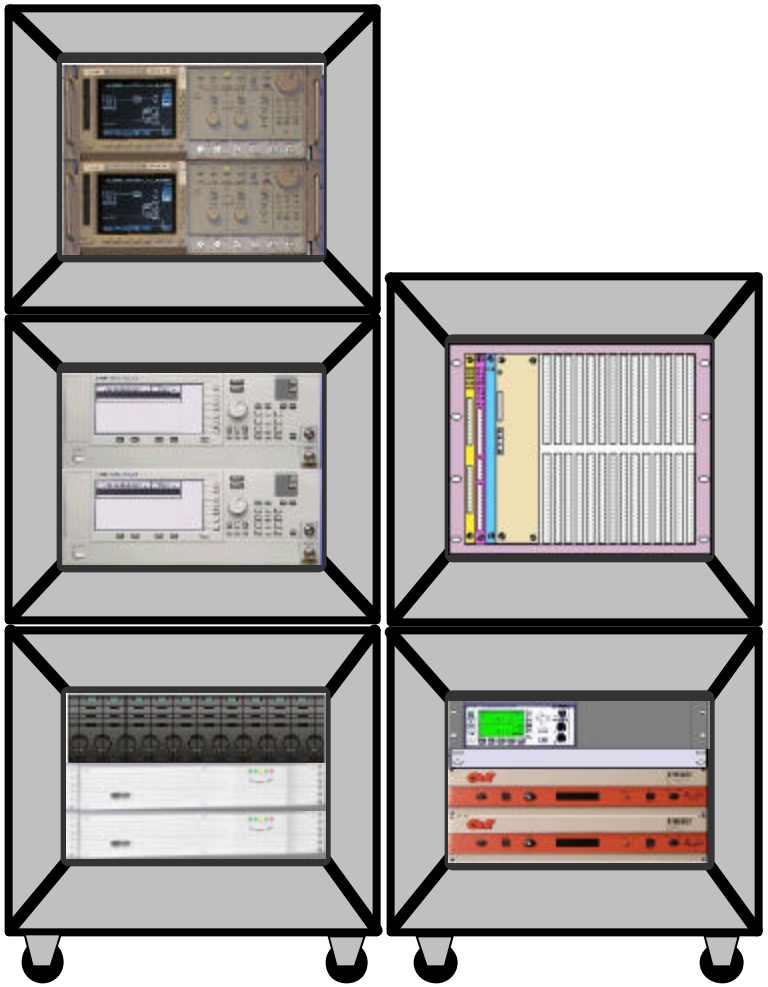
AOP2 Hardware Configuration*

Waveform generators
- **Reference**
- **Return**

Programmable LOs for tunable RF front-end

Real-time file system

UPS



6U card cage
- Controller card
- Optical module
- Post processing & Timing card

Power Meter

RF module

Power amplifiers

* Including test equipment

AOP Production Conceptual Configuration

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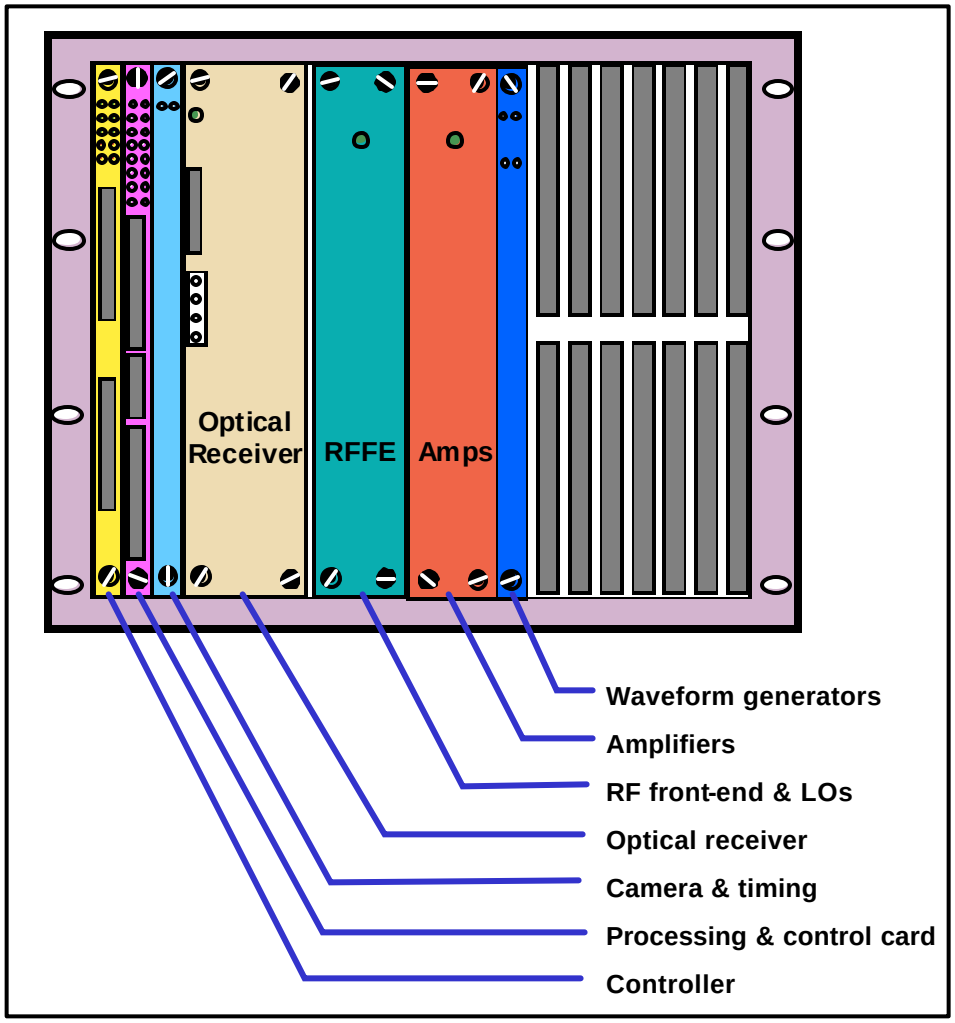
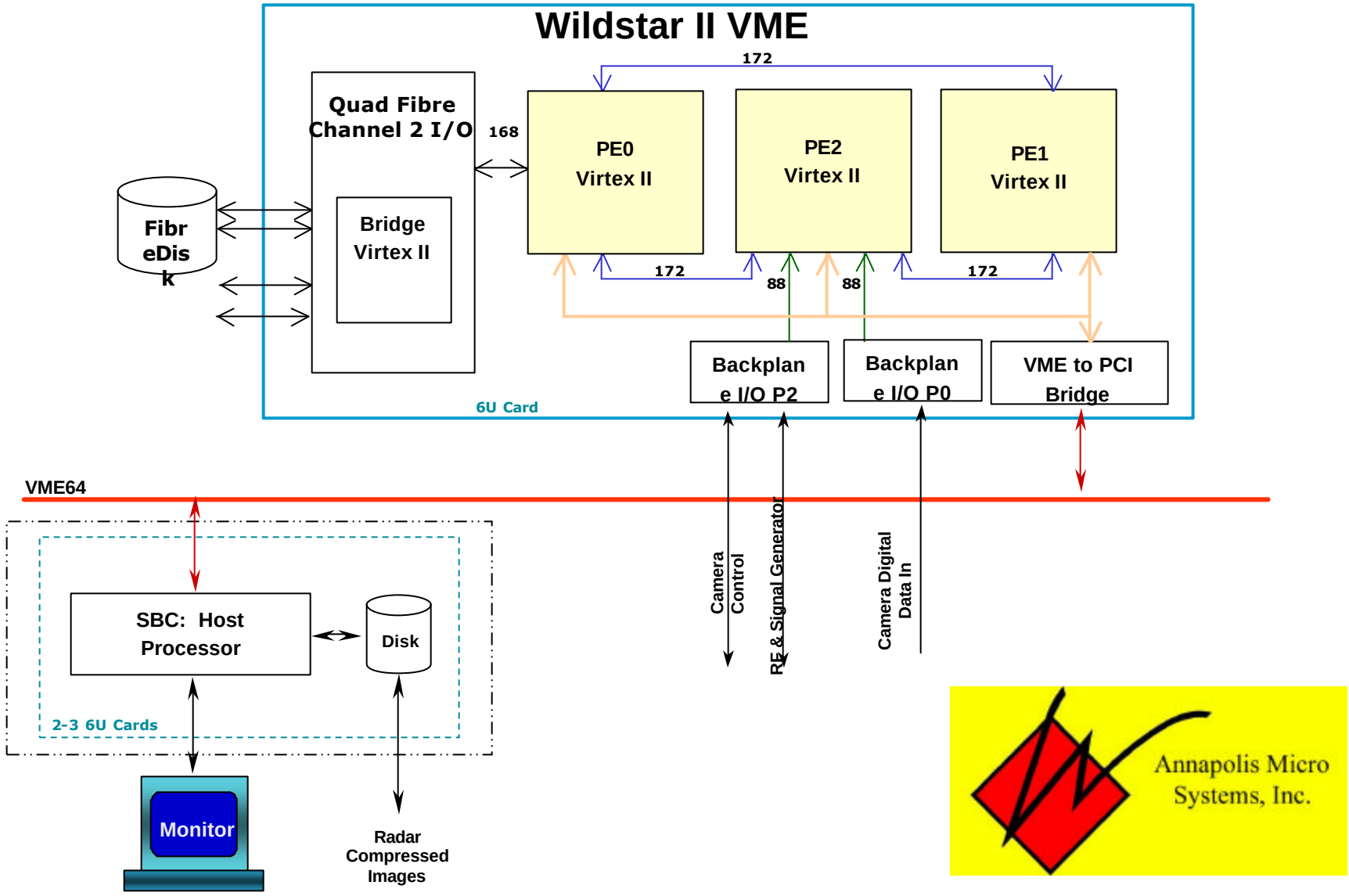
Size reduced from ½ rack in AOP2 demonstration to ½ single 6U chassis:

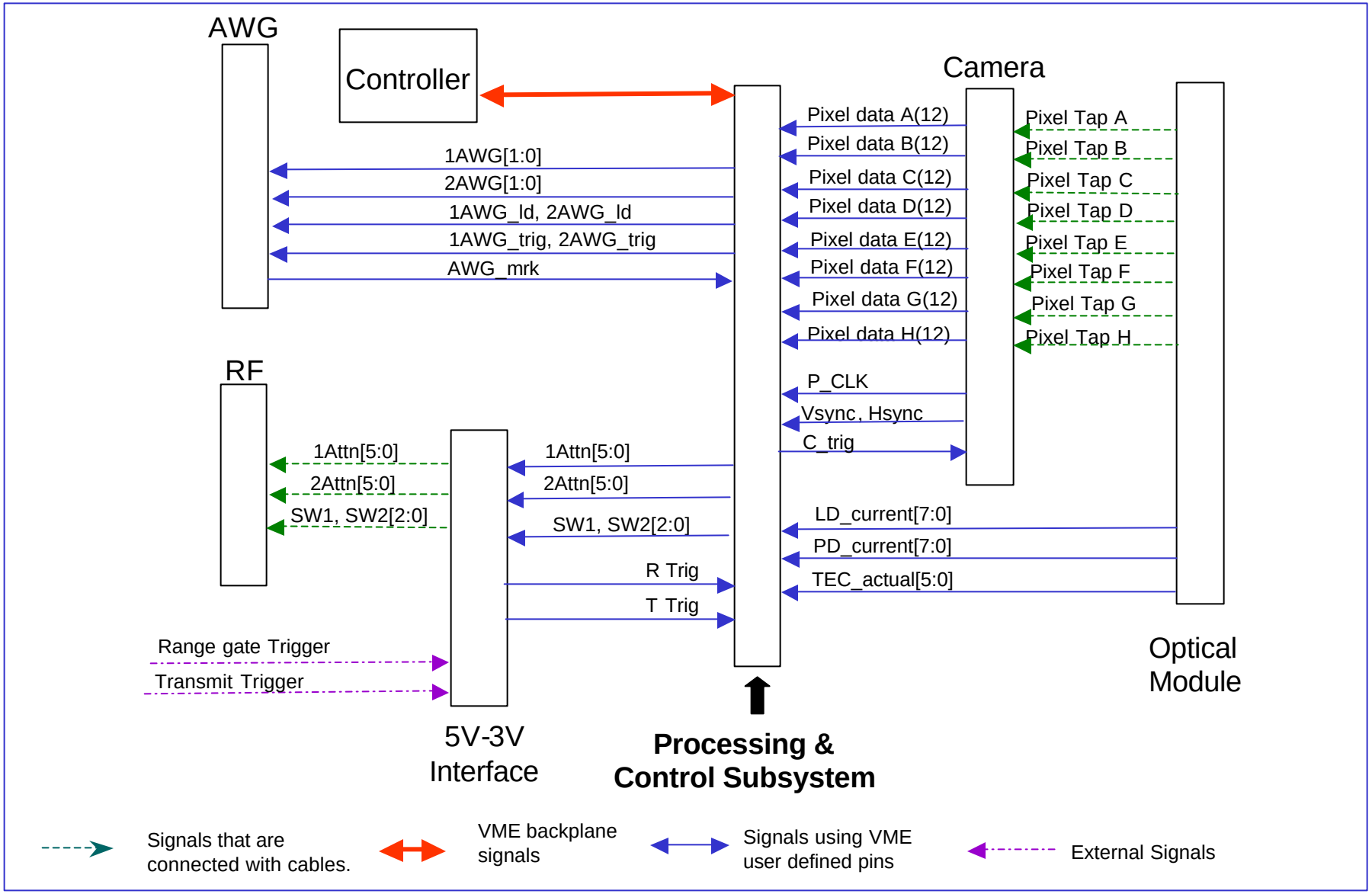
- **AWGs reduced to single chip for PRN codes**
- **Synthesizers reduced to fixed LOs**
- **Amplifiers reduced to single card**
- **No output data storage, data sent to radar post processing in real time**



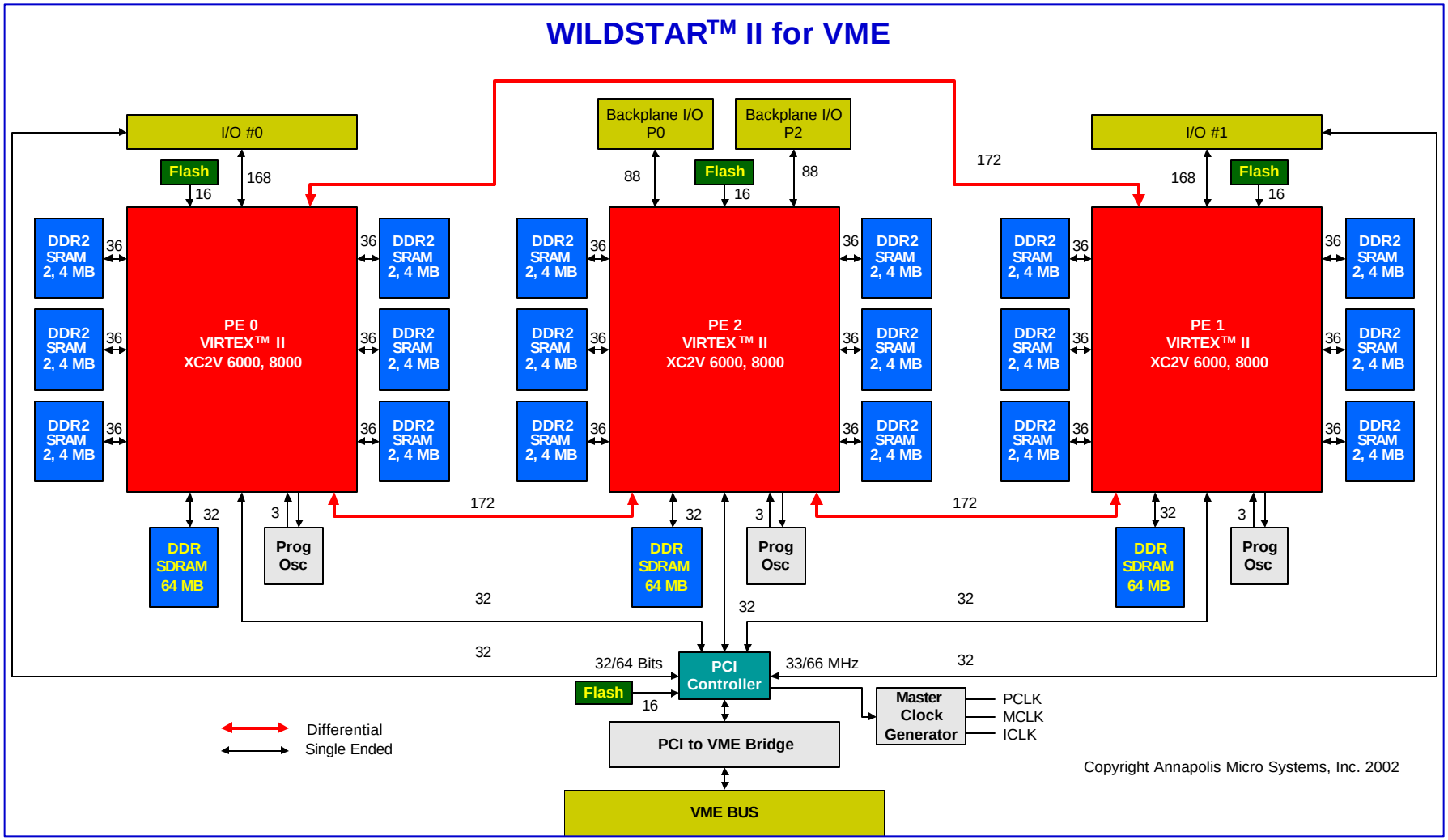
Post Processing & Control Subsystem (PCS)



PCS External Interfaces



FPGA based reconfigurable computing board



WILDSTAR™ II for VME & Fibre Channel 2 I/O Card

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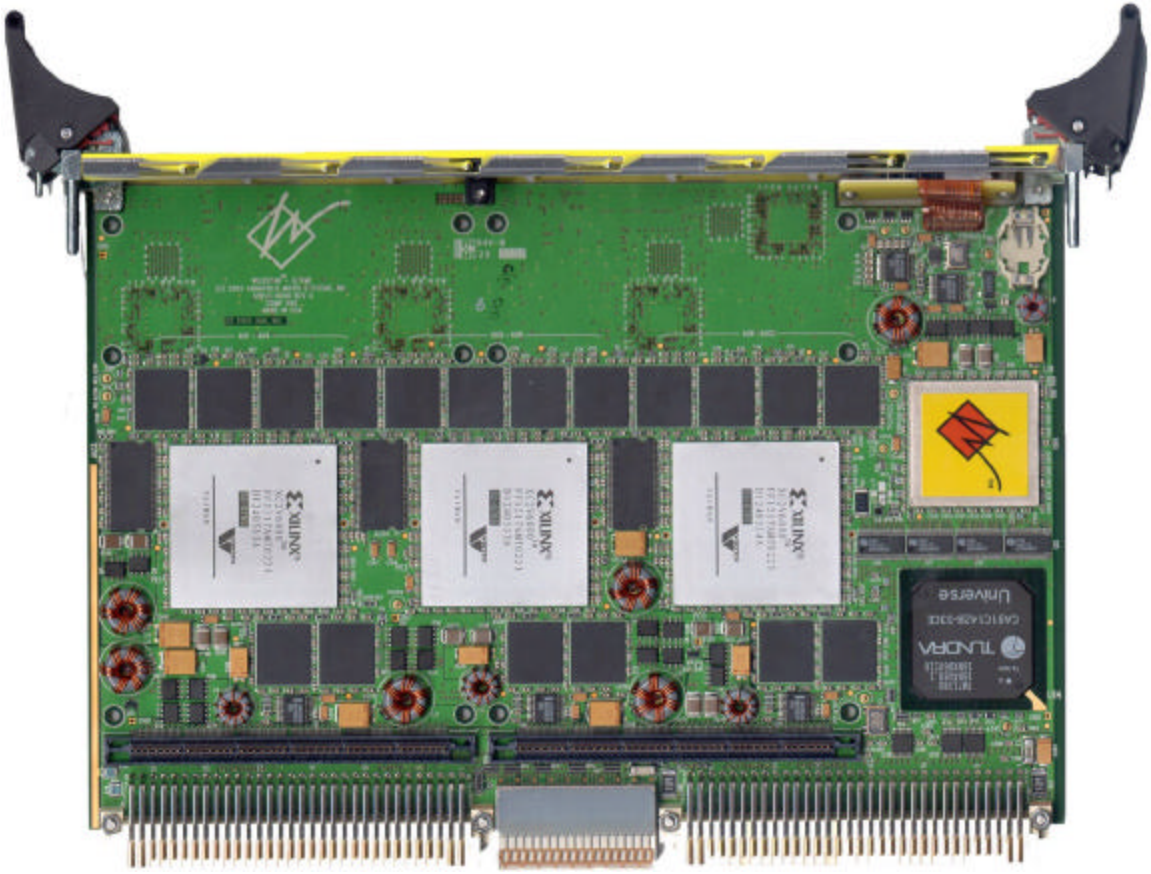

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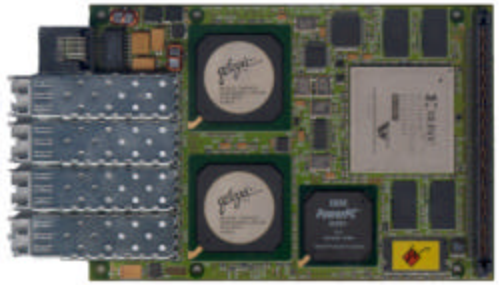
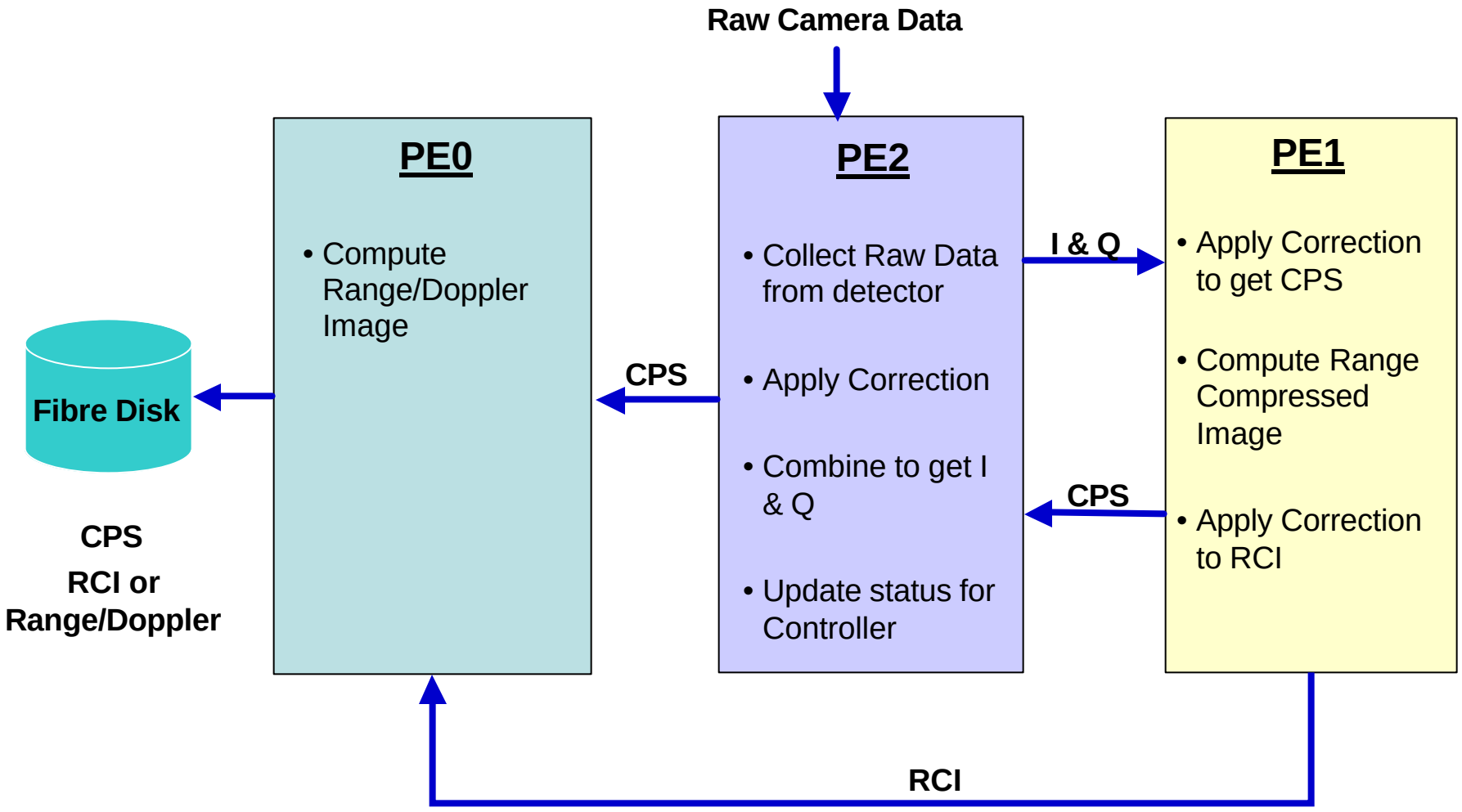


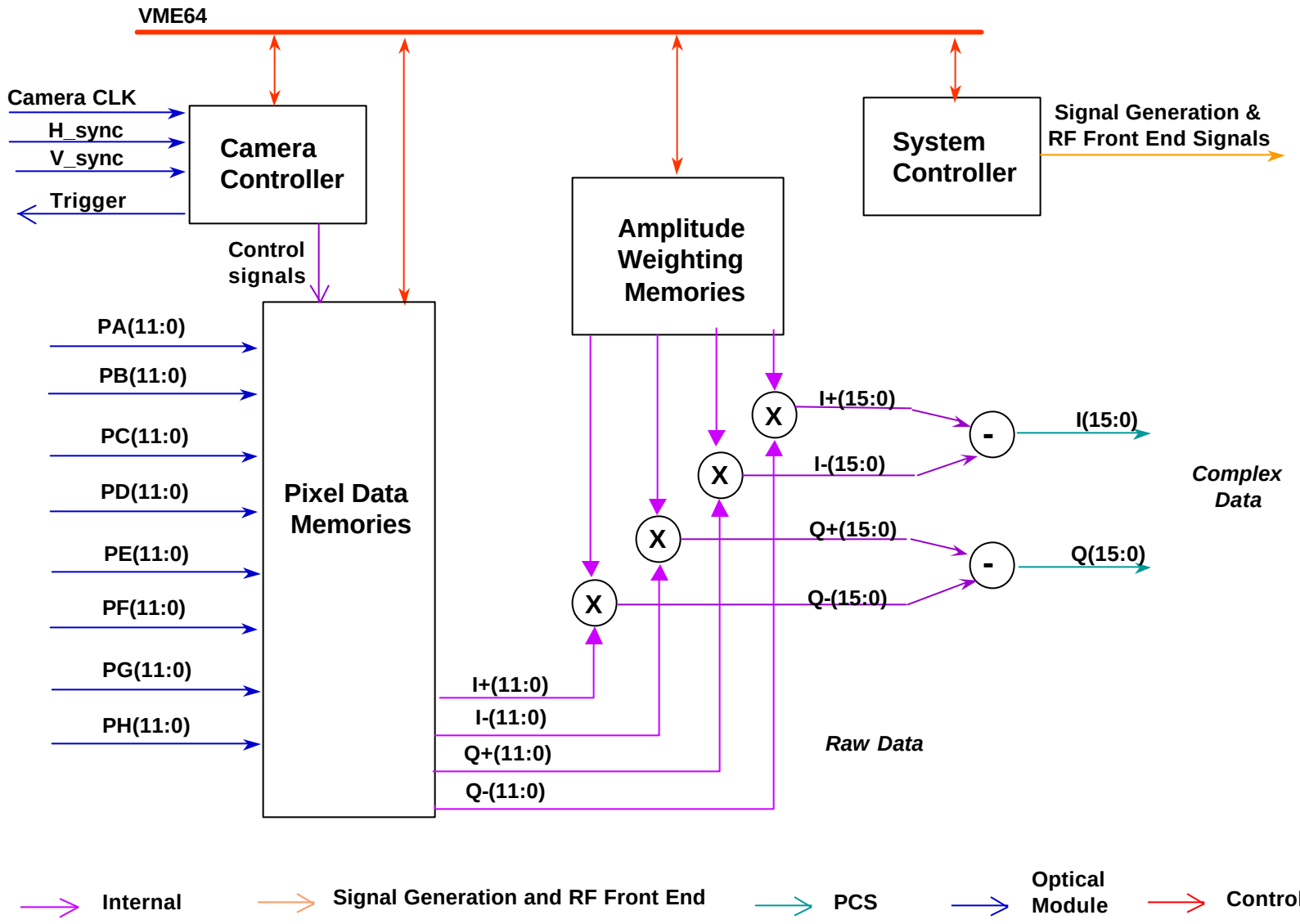
WILDSTAR™ II FPGA card

Fibre Channel 2 I/O Card daughter card

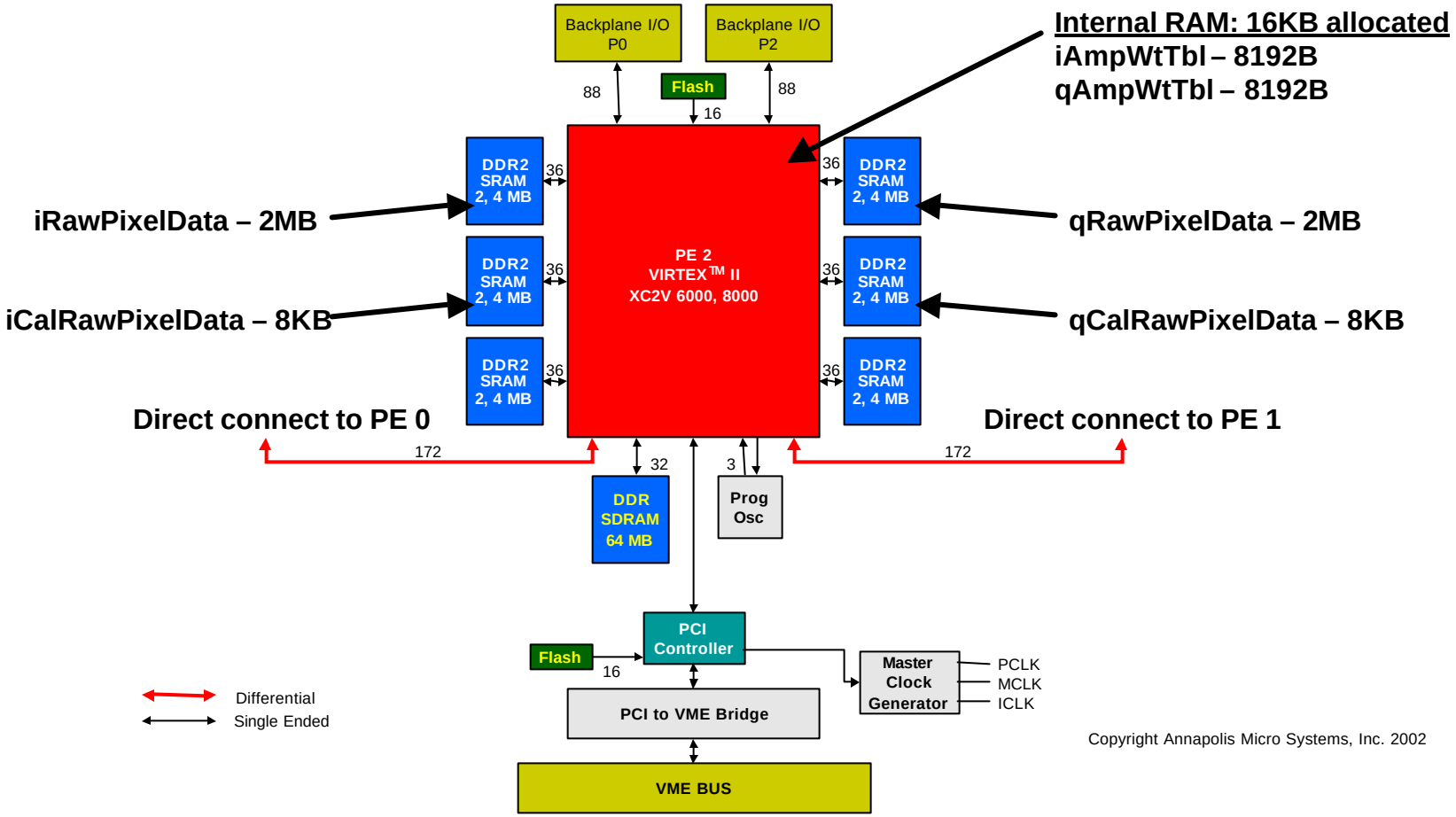
Internal PCS Interfaces



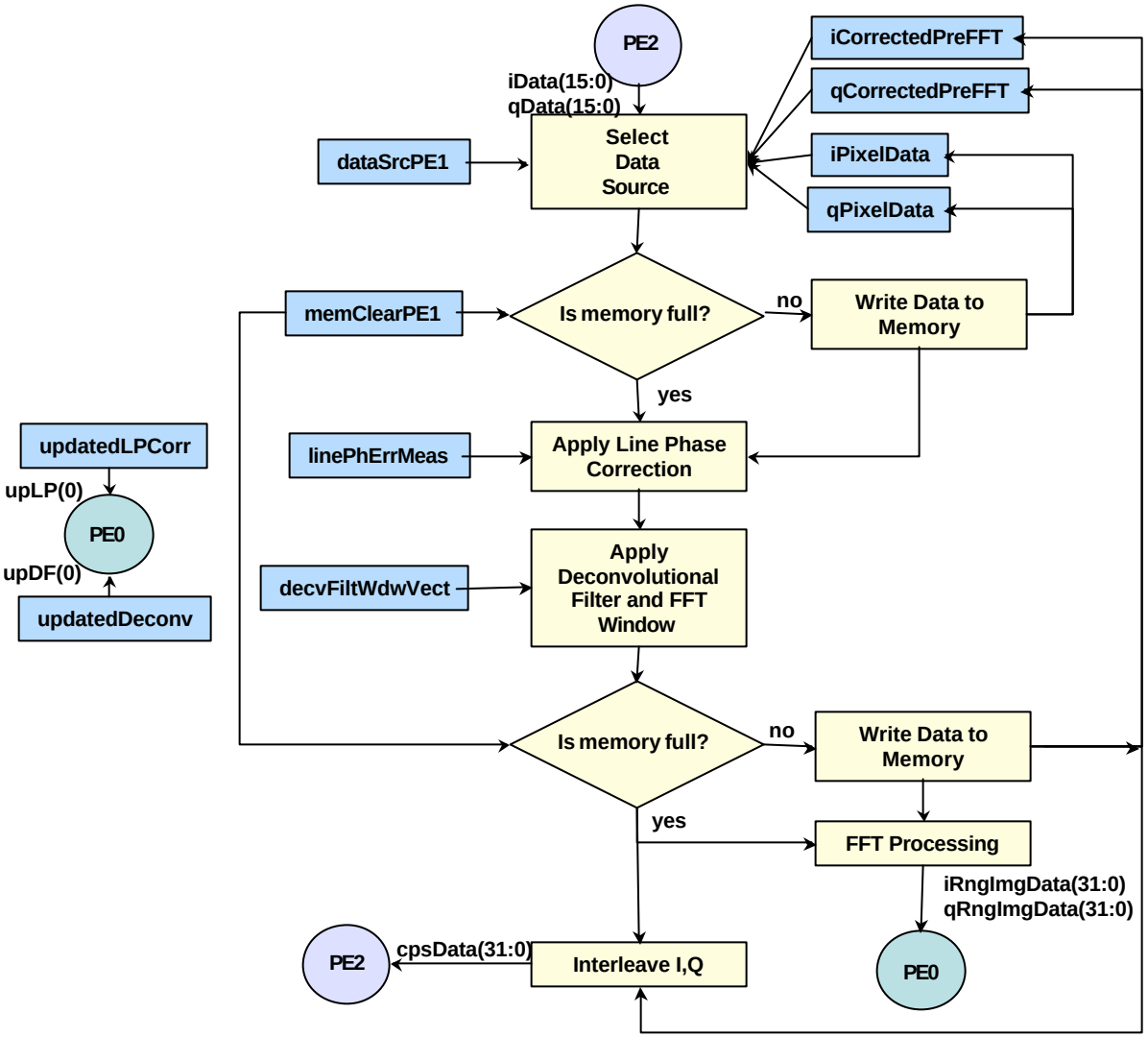
PE2 Data Processing



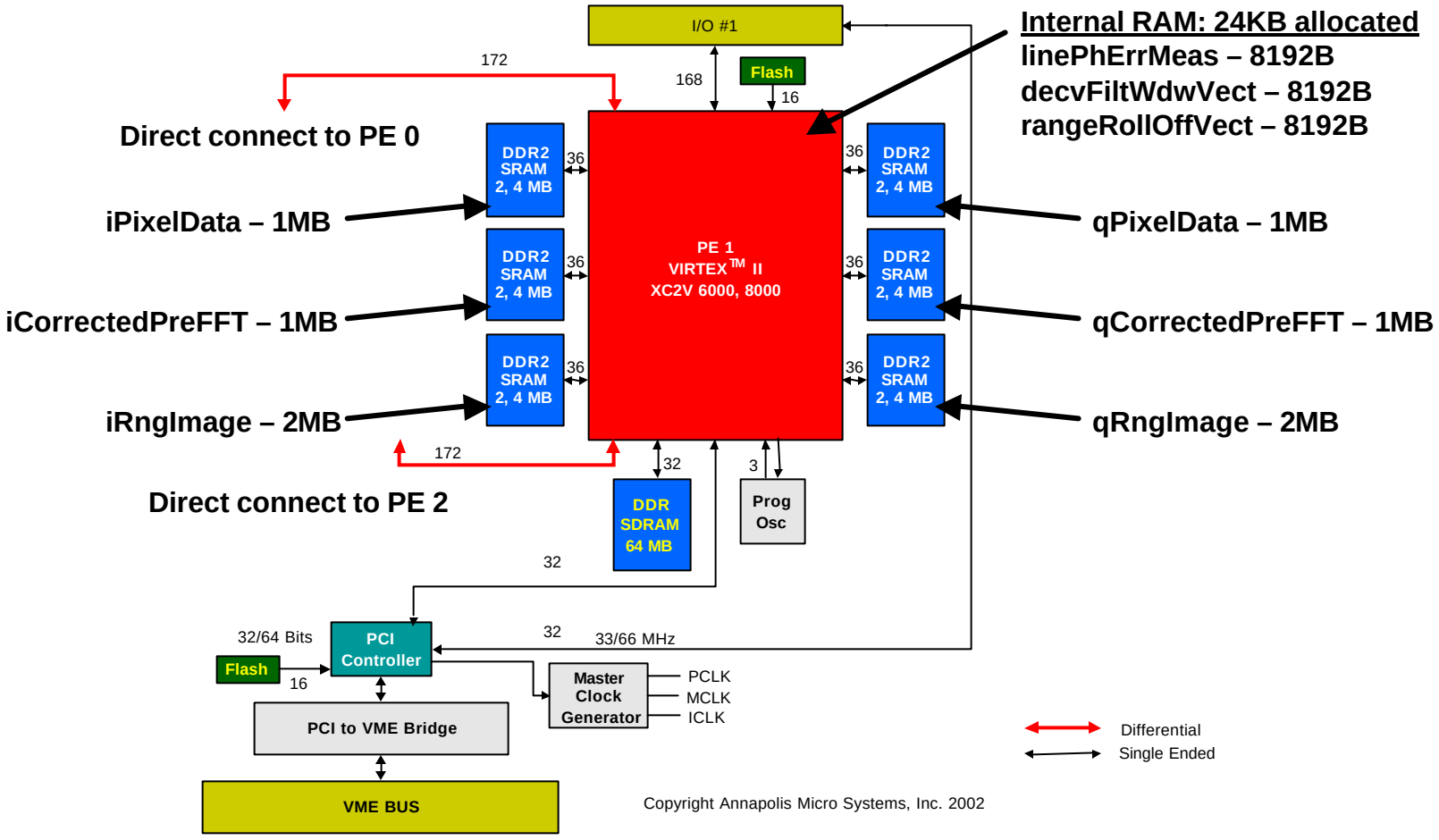
PE2 Allocated Memory Diagram



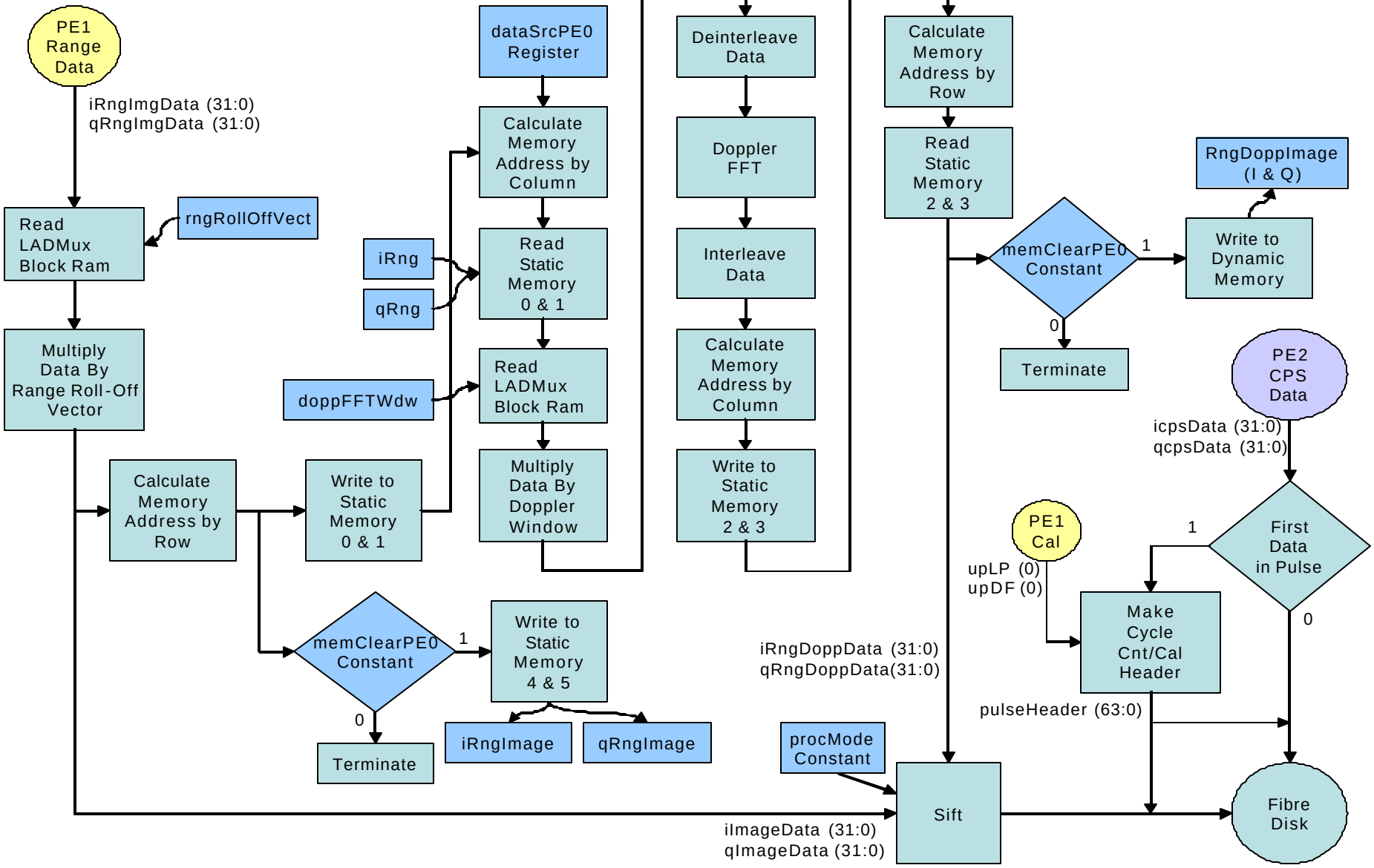
PE1 Functional Flow Diagram



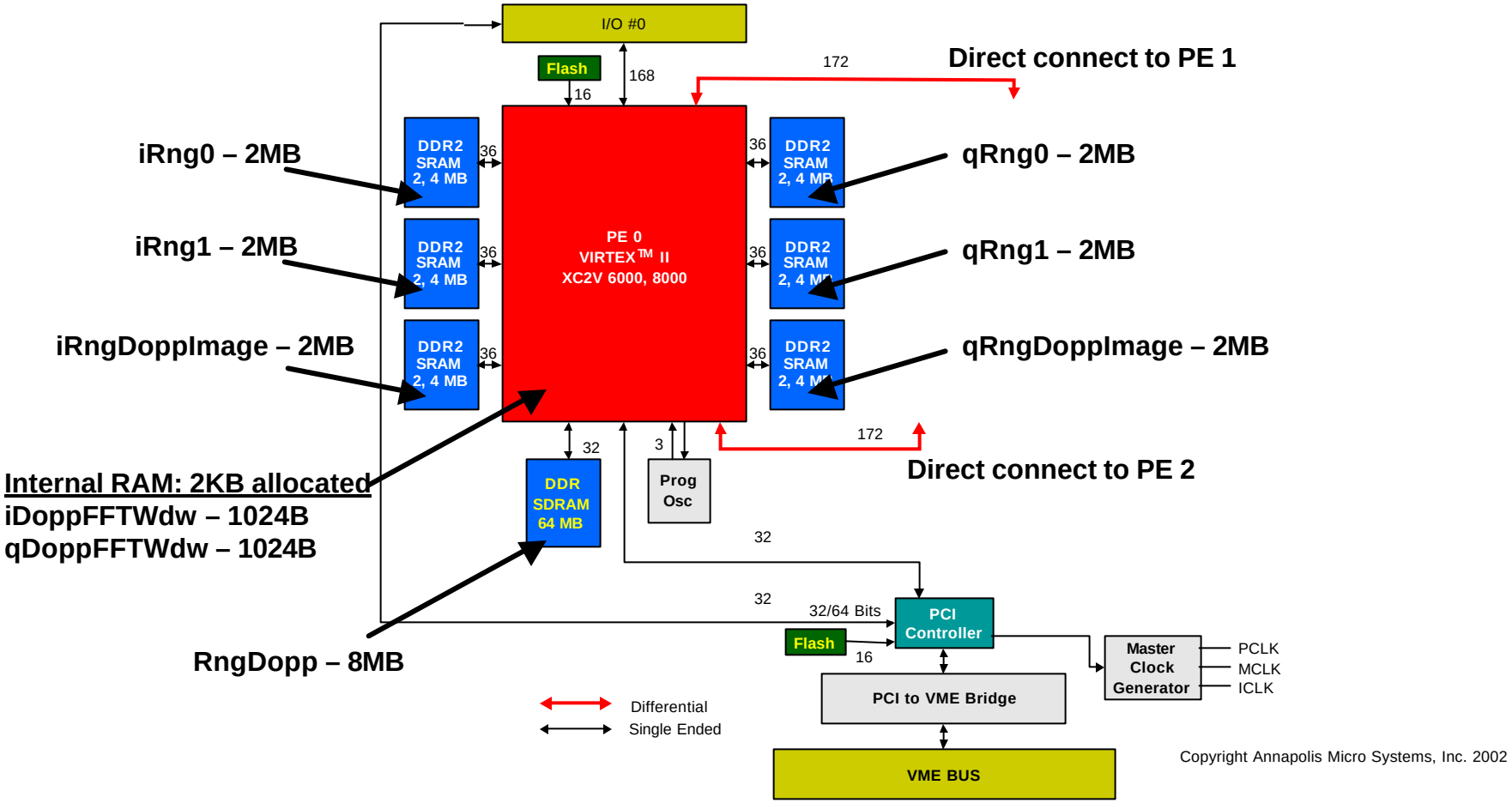
PE1 Allocated Memory Diagram



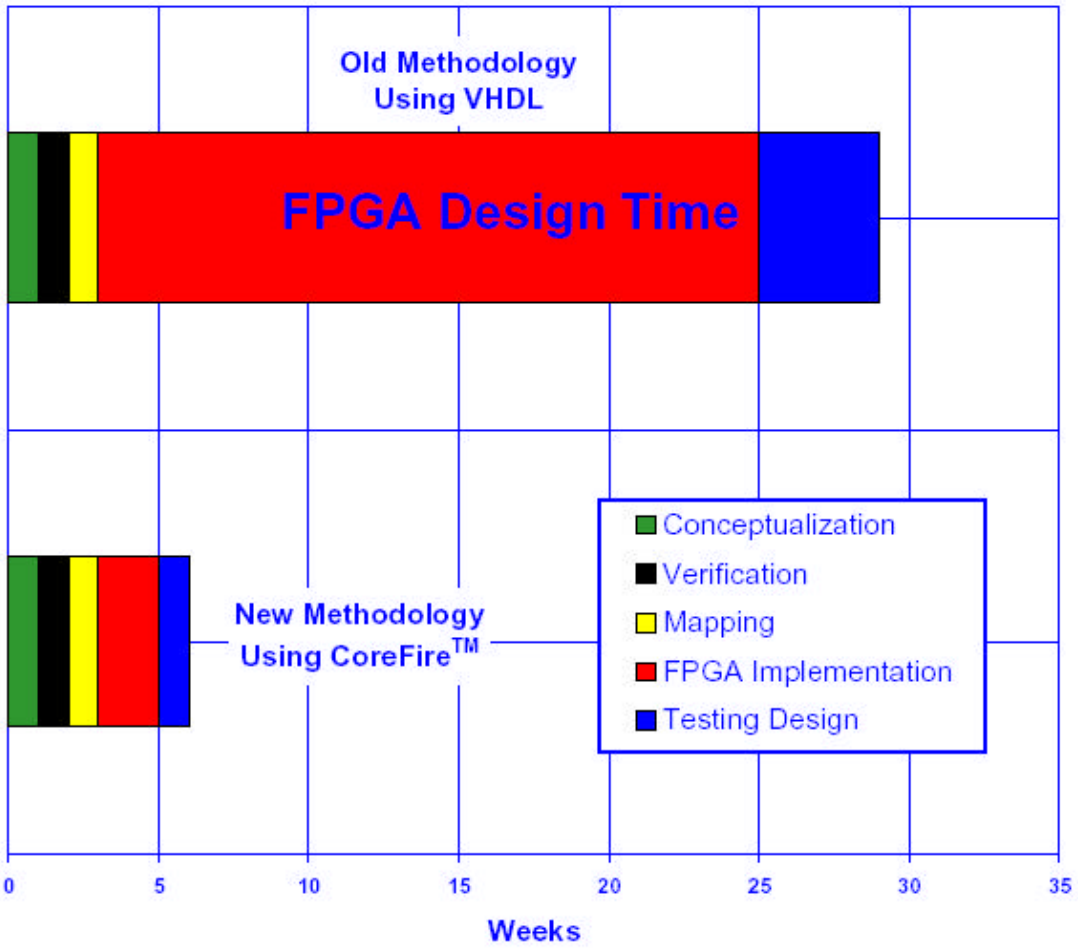
PE0 Functional Diagram



PE0 Allocated Memory Diagram



FPGA Design Time: CoreFire™ vs. VHDL



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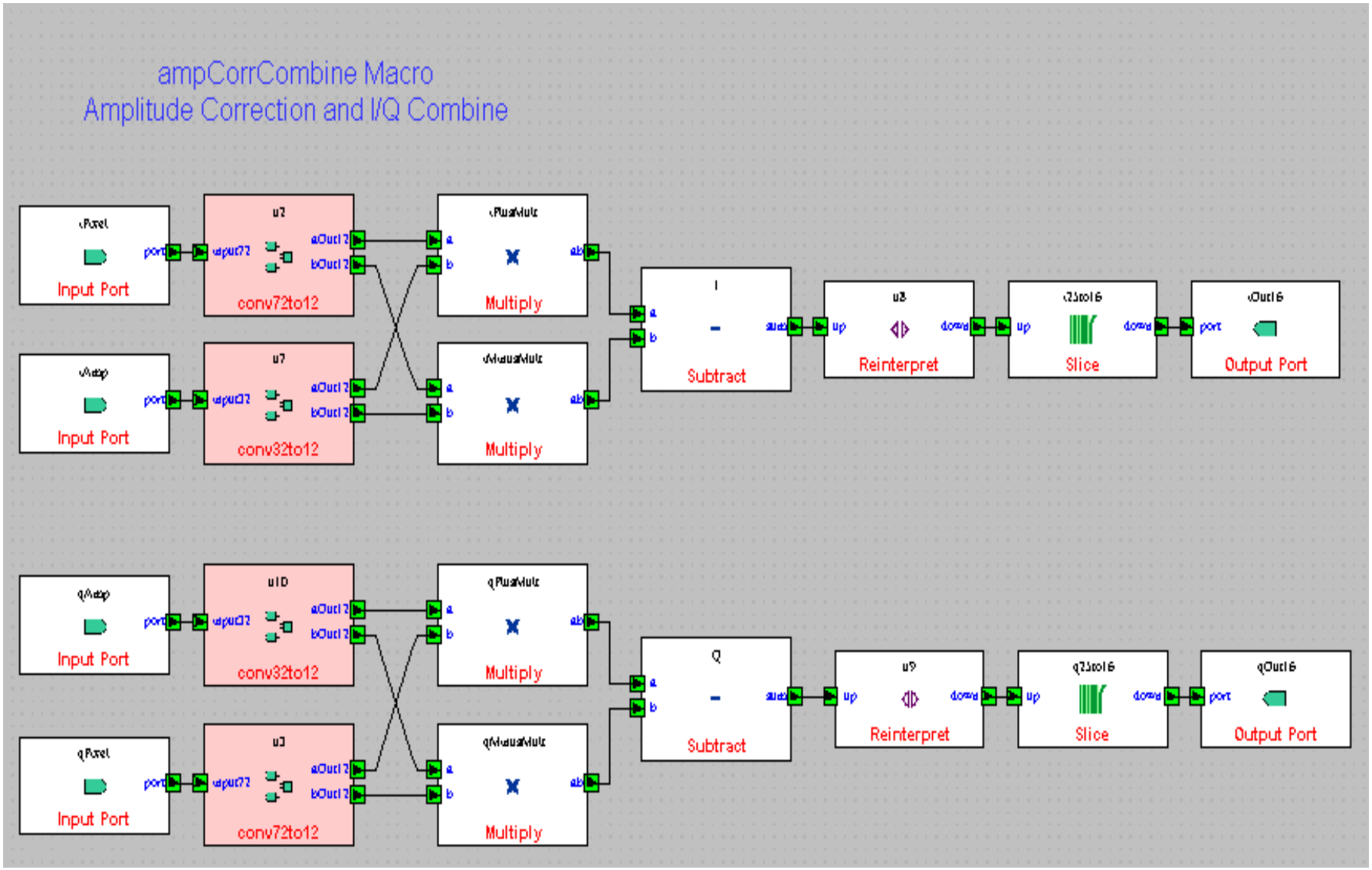
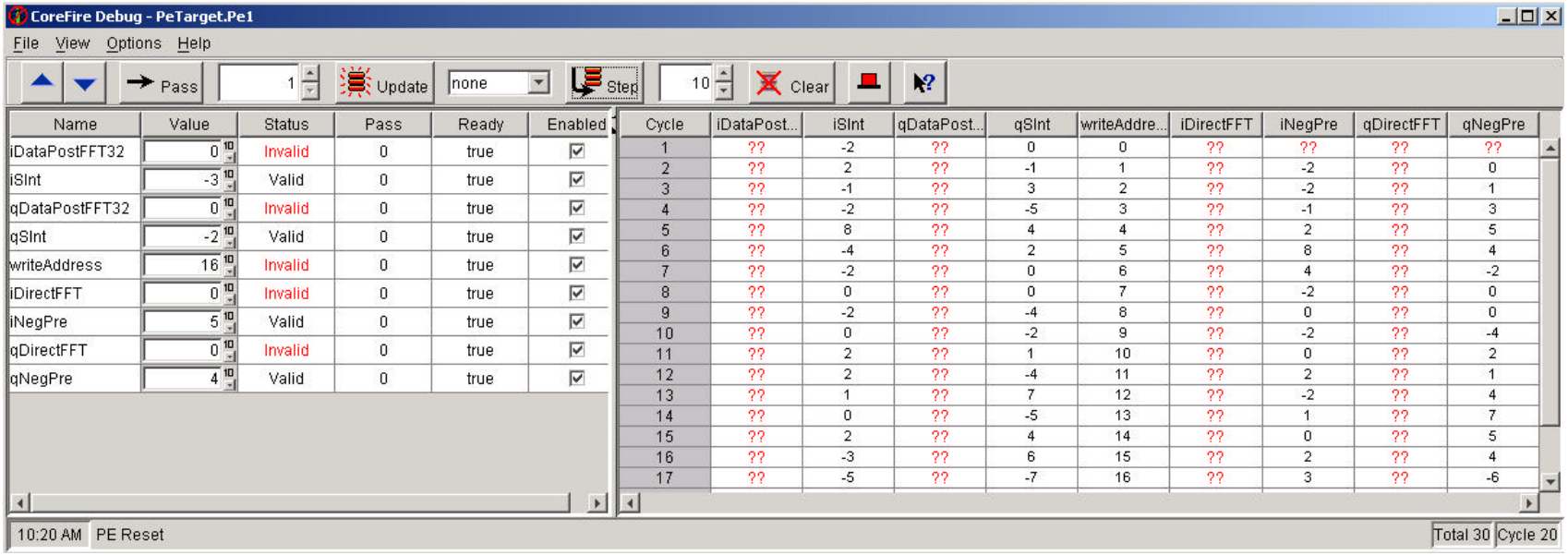
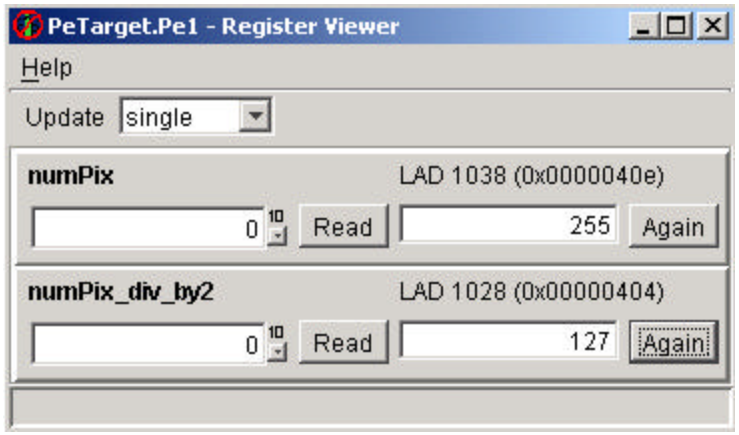
Corefire Example

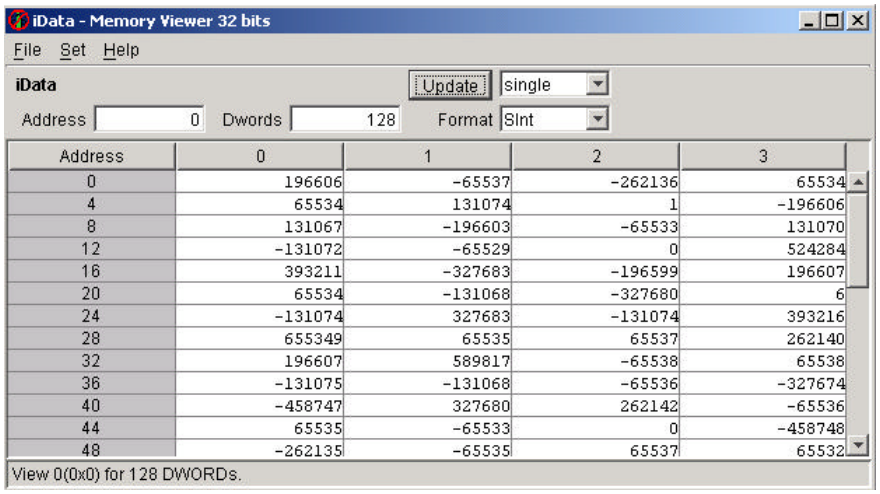


PCS Testing: CoreFire Debugger

CoreFire™ Application Debugger includes windows for monitoring and manipulating data flow







Wildstar II FFT Example

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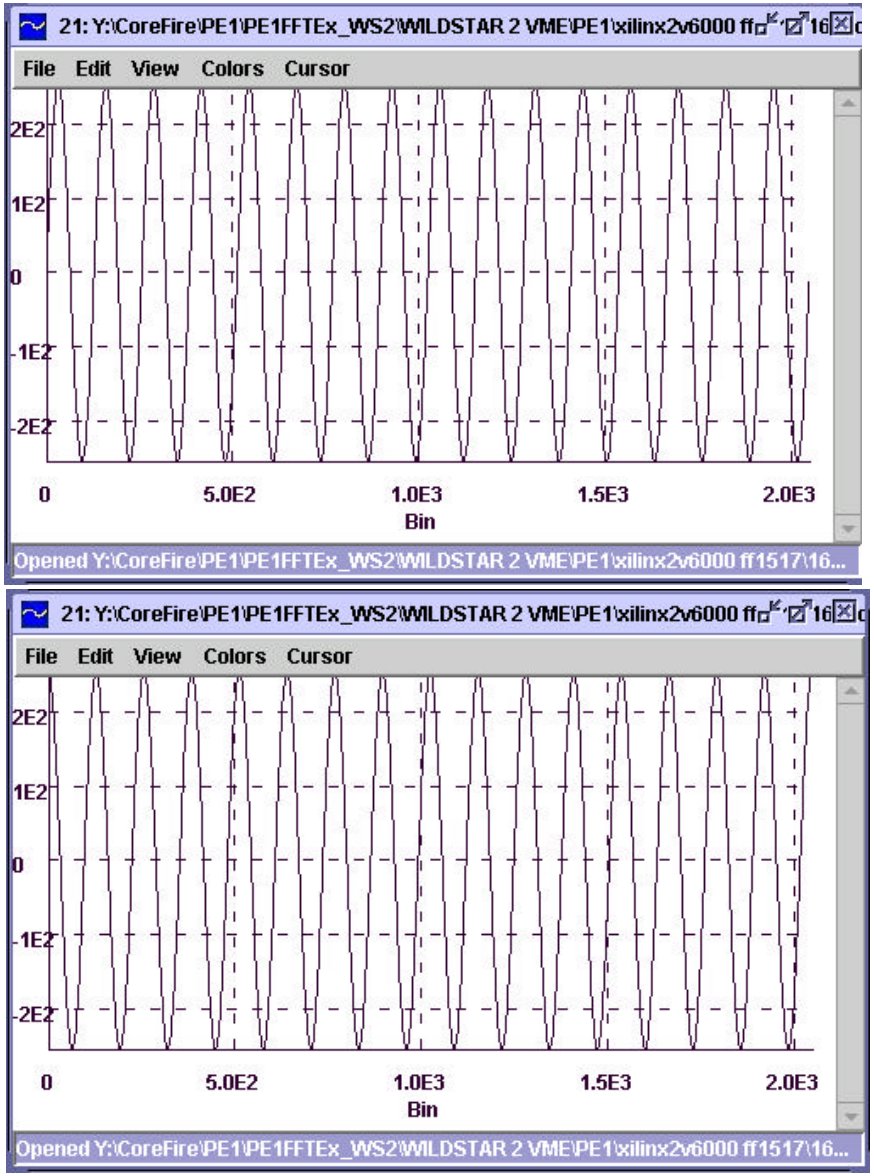
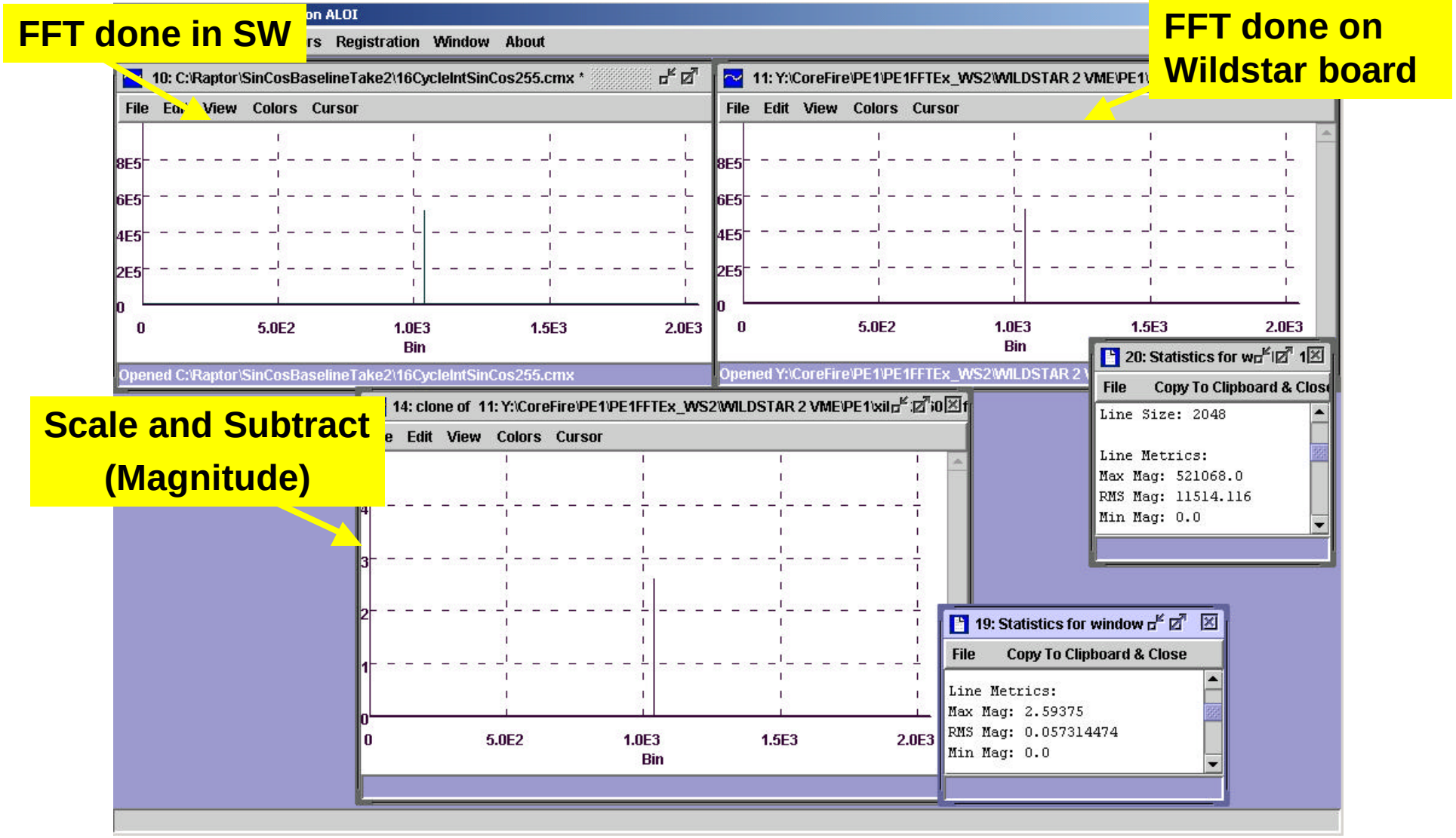
FFT Example Scenario

- **CoreFire project for PE1**
  - Data read from memory on Wildstar II board
  - FFT operation
  - Data written to memory on Wildstar II board
- **Java program**
  - Data read from file
  - Data written to memory on Wildstar II board
  - Data read from memory on Wildstar II board
  - Data written to file
- **CoreFire Debugger**
  - Kicks off the Wildstar II board processing
  - Memory and register viewers show data during the processing
- **IView Tool**
  - Compare output data file with expected results



Wildstar II FFT Example



Peak to RMS = 139 dB

Conclusions

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- **Essex has been able to implement an extremely complex, computationally intensive radar processing task in:**
  - **Embedded optical hardware and**
  - **Embedded DSP/FPGA hardware**

- **This approach saves space, development time, software, development costs and maintenance costs.**

- **The AOP hardware allows the use of new arbitrary classes of waveforms for improved ballistic missile discrimination.**

Wrap-up / Questions