Session 4: Reconfigurable Computing

Session Chair: David Cousins
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It's always been about *Performance*

- "Civilization advances by extending the number of important operations which we can perform without thinking."

  Alfred North Whitehead (1861 - 1947) Introduction to Mathematics (1911)

- "Never promise more than you can perform."

  Publilius Syrus (~100 BC), Maxims

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Increasing performance is the common thread in this session

- Increasing Performance with Reconfigurable Computing through:
  - Algorithm decomposition
  - Arithmetic bit-width manipulation
  - A new SIMD on-a-die architecture
  - Morph-able computing architecture
  - *Stability* across multiple kernels and data sizes

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Custom Reduction of Arithmetic in Linear DSP Transforms

Smarahara Misra, James C. Hoe, Markus Püschel, Electrical and Computer Engineering, CMU

- Performance through algorithm decomposition
- Defines a process for generating cost optimal multiplier-less algorithms with SPIRAL
  - Manipulate SPIRAL output to increase numerical stability
  - Use constrained optimization to reduce the number of operations while still satisfying quality threshold
    - Evolutionary and greedy search algorithms
  - Map to Verilog
- Presents experimental results: DCT8 and DFT16

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Precision Modeling and Bit-width Optimization of Floating-Point Applications

Zhihong Zhao, Alternative System Concepts
Miriam Leeser, Northeastern University

- Performance through bit-width manipulation
- Optimal FP bit-widths are the smallest bit-widths that satisfy accuracy requirements.
- Apply an FP precision modeling approach
  - Avoids computational intensity of simulation-based approaches
  - Models takes the form: error = f(op, bit-width)
  - Models are built by profiling a Control and Data Flow Graph of the application
  - Application Precision model is then optimized using Grid Steepest Descent

An Ultra-High Performance Architecture for Embedded Defense Signal and Image Processing Applications

Stewart Reddaway, Pete Rogina, WorldScape Defense Co.
Ken Cameron, Simon McIntosh-Smith, David Stuttard, ClearSpeed Tech.
Michael Koch, Rick Pancoast, Joe Racosky, Lockheed Martin

- Performance through a new SIMD processing architecture:
  - –Multi-Threaded Array Processor
  - –Array of processing elements on a single die.
  - –Packet switched bus architecture
- HPEC application performance benchmarks
  - –Cycle-accurate simulator

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DARPA PCA for Embedded Defense Signal and Image Processing Applications

Michael Koch, Joe Racosky, Mike Iaquinto, Rick Pancoast, Lockheed Martin
Steve Crago, Matt French, University of Southern California

- Performance through morphable architectures
- Describes an embedded processing application
  - Radar waveform signal processing
  - Architecture morph
  - Non-coherent integration processing
- Processing functions:
  - Radar pulse compression, magnitude computation, range-walk compensation, and non-coherent integration
- Benchmark results compare conventional PowerPC, PCA simulation, and actual PCA hardware

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Kernel Benchmarks and Metrics for Polymorphous Computer Architectures

James Lebak, Hank Hoffmann, Janice McMahon; MIT Lincoln Laboratory

- Performance measurement across seven kernel benchmarks
  - Considerable variation in throughput
  - *Stability* ? Minimum/maximum throughput
- A chief goal of PCA is for stable performance across a range of kernels and data sizes.
- Presents performance results for several kernels on the MIT RAW simulator

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Invited Speaker: Robert Graybill

Program Manager DARPA IPTO

Data Intensive Systems,
Power Aware Computing and Communications,
Polymorphous Computing Architectures,
High Productivity Computing Systems

Topic: Are we adrift in the sea of COTS?

- Review HPEC technology directions from an historical perspective
  - DARPA ITO-IPTO and MTO
- Future suggestions