

# *HPEC 2003 Workshop*

## *Session 1: New Challenges and New Architectures*

Session Chair: David Cousins

Division Scientist

High Performance Computing Dept

BBN Technologies

**BBN**  
TECHNOLOGIES  
A Verizon Company

# Counter Terrorism Technology Challenges (1)

1. Pattern matching of streams at Tb/sec rates
2. Concept transformation and analysis technology
  - Engineering dynamic, overlapping, federated ontologies
    - Pruning, segmentation, decomposition, and re-aggregation
  - Convert concepts into pattern match templates
3. Manipulating Data as Networks and Graphs (huge ones at that)
  - Need techniques to discover and describe patterns of interest within extremely large graphs

# Counter Terrorism Technology Challenges (2)

4. Accurate machine translation of raw data such as images, video, handwriting, foreign language speech etc.
  
5. Context Aware Visualization
  - Enable people to monitor, understand, and interact with system activities at multi-terabyte rates
  - Visualize abstracted concepts, transforms, and feature spaces
  
6. System architectures
  - How to design, build, and control massive systems?
  - System metrics and performance characterization



*Invited Speaker: Dr. Ruth David*

President and CEO,  
ANSER Institute for  
Homeland Security

*Topic:* Homeland Security:  
Challenges for the Computing  
Community

# The Mercury System: Embedding Computation into Disk Drives

*Roger D. Chamberlain, Ron K. Cytron, Mark A. Franklin, and Ronald S. Indeck; Center for Security Technologies, WUSL*

- *Problem:* Data Searches in a conventional systems result in inefficient use of fast components.
- *Solution:* embed a reconfigurable search engine directly in the disk drive. Enables unstructured text searching and sequence matching at full streaming disk rates
- *Future efforts:*  
Image search  
template matching

Table 1. Application speedups.

Application	Disk-limited speedup	Logic-limited speedup
Exact text search	1.1	14
Approx. text search	12	31
Biosequence search	50	125

# Hybrid Optical/Digital Processor for Radar Imaging

*Mr. Keith Frampton, Essex Corporation;*

*Mr. Patrick Stover, Annapolis Micro Systems, Inc.*

- *Presenting a case study:*
  - Integration of optical and COTS FPGA technologies.
  - Accelerated development through the use of COTS FPGA application builder tools.
  - Processes 1 GHz of instantaneous bandwidth in real time without wide band ADCs.

# HPCS Application Analysis & Assessment

*Dr. Jeremy Kepner, MIT Lincoln Laboratory*

*Dr. David Koester, The MITRE Corporation*

- ***Problem:*** How do we assess the end-user value of new “high productivity” computing systems for a given mission?
  - Must move beyond the “MachoFlop”.
  - Reassess how one defines and measures:  
performance, programmability, portability,  
robustness and productivity.
- ***Solution:*** HPCS is developing an assessment framework where both *Execution Time* and *Development Time* are quantified in order to measure overall Productivity