Successful VSIPL Software Application Migration

A Case Study: NATO SEASPARROW Illumination Radar Signal Processing

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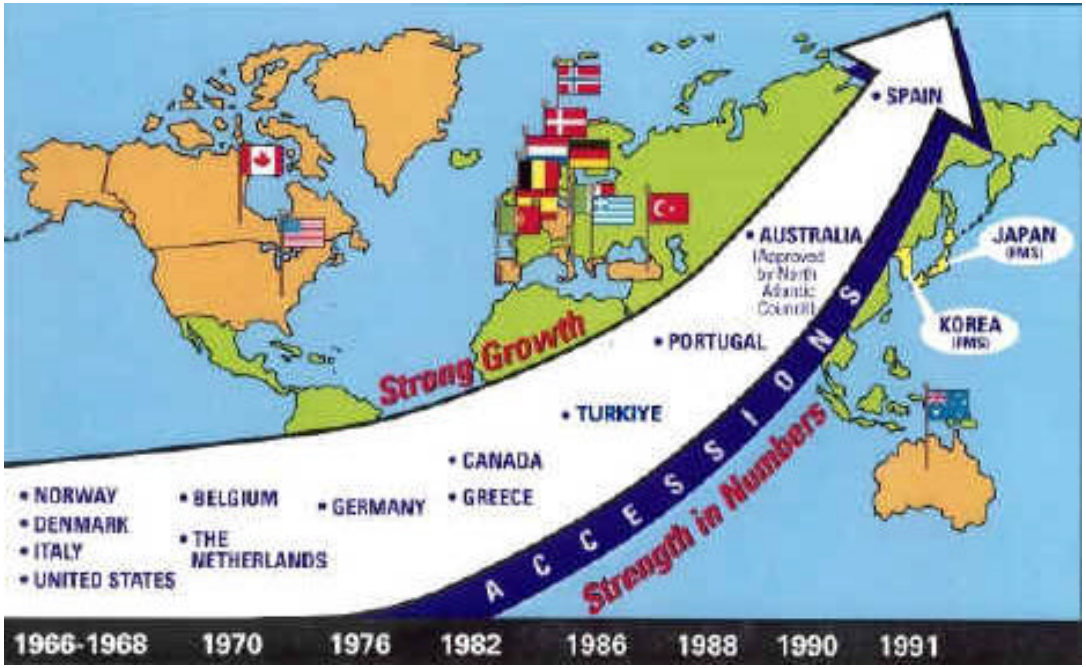
Sponsor Information

- NATO SEASPARROW Project Office
  - NATO's Largest And Most Successful Cooperative Weapons Project
    - (18 partici-pating or user governments)



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VSIPL Application Migration

- Application Characteristics
- Justification
- Migration Strategy
  - Port In Place To VSIPL
  - Port VSIPL Application To Alternate Platform
- Process Detail
- Results And Experiences
- Costs And Benefits
- Observations On VSIPL
- Observations On Migration

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Application Characteristics

- 10 GHz Continuous Wave Illumination Radar Signal Processing Software
- 140 KHz Bandwidth Of Interest
- 43 Hz Iteration Rate
- 7:1 FIR Decimation Of Digitized Time Series
- Two 4K FFTs
- Several 64 Point Inverse And Forward FFTs
- Analyze AM and FM Signal Components To Produce Tracking Data Products

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Hardware Platforms

- Existing Platform
  - Sky Computers SkyBolt II Excalibur Hardware
  - Vector Processing Implemented On Sky Standard Math Library
  - Software Is Tested And Deployed Aboard Surface Combatants
- Target Platform
  - Motorola MVME5110 (MPC 74xx) Hardware With Echotek GC214 DDR
  - MPI Software Technology VSI/Pro VSIPL

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Software Application Metrics

- 10K Source Lines Of Code
- 15% Comment
- 26 Source And Header Files
- 300 Calls To Vector Library
- 65 Unique Vector Functions Used

- Not Strictly A "Metric", But Application Made Liberal Use Of extern Statement For Data Structure Access

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Justification For Migration

- NSPO Requires Additional Copies Of Deployed System
  - Existing Platform Includes COTS Products No Longer Available
  - Replacement COTS Processing Capacity Far Exceeds Application Requirement
- Significant Programmatic Investment In Signal Processing Algorithms
  - Development
  - Verification And Testing
  - Ongoing Algorithm Enhancement
- VSIPL Available On Several COTS Computer Platforms
  - Permits Competitive Hardware Cost / Performance Evaluation
  - Future Software Upgrades Portable To All Installations

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Risk Reduction Migration Strategy

- Port In Place To VSIPL
  - Sky Computers Provides Correct And Complete VSIPL Implementation As A Layer Over Sky Standard Math Library
  - Verify Port Correctness On Legacy Hardware
- Port VSIPL Application To Alternate Platform
  - Verify Equivalent Results On New Target Hardware

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Iterative Real Time Software Constraints

- VSIPL "Create" and "Destroy" Verbs Not Available To Iterative Software
  - Heap Fragmentation Causes Indeterminate Execution Time
  - All "Create" And "Destroy" Calls Confined To Initialization
- Compels The Cataloguing Of Objects Implied By The Existing Code
- Requires Initialization Code To Create Each Needed Object With Proper Scope

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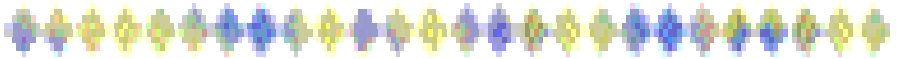
The Persistent Object Management Challenge

- Vector Offsets, Lengths, And Strides
  - Were Freely Specified As Function Arguments
  - Now Carried As View Object Attributes
  - Forces Evaluation Of Memory Block Utilization: Need For Different Simultaneous Views Of Any Memory Block
  - Forces Coherent Policy On Attribute Persistence
- FFT Objects
  - Forward, Reverse
  - In-Place, Out-Of-Place
- FIR Filter Objects
- Chebyshev Weight Objects
- Real And Imaginary Derived Views Of Complex Vectors



- Most Conversion Coding Errors Will Be Found In View Attributes

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Steps To Port In Place To VSIPL

1) Catalog Existing Vector Library Calls
   - Link Without The Vendor Library
   - Compile Without The Vendor Header File
2) Map To Functionally Equivalent VSIPL Calls
   - Solicit Vendor Mapping
3) Address Surprises And Subtleties
   - FIR Filter
   - Inverse FFT
4) Confront The Object Management Challenge
   - Catalog Vector Memory Buffers Used In Legacy Application
   - Catalog Distinct Offset And Stride Combinations
   - Identify Vector Data Types / Precisions In Use
   - Catalog High Order Process Objects
     - FFTs
     - FIR Filters
     - Chebyshev Weights
   - Identify Scope Of Use

Steps To Port In Place To VSIPL (continued)

5) Add Initialization Functions Throughout Application
   - Create Or Pass Address(es) Of Required Objects
6) Implement VSIPL Function Call Mapping
   - Use Conditional Compilation Switches So VSIPL Calls Are Side-By-Side With Legacy Calls
   - Instrument For Formatted Vector Capture At Manageable Source Interval
   - Pay Special Attention To View Attribute Values (offset, length, stride)
7) Compile Clean With And Without VSIPL Switch
8) Test And Verify Numeric Results
   - Correct Errors
   - Iterate Until Accurate
9) Strip Legacy Source And Compilation Switches Out Of Implementation
10) Deliver

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Inverse FFT Before And After

```
ccopy(VECSZ,
  psTemp, 1,
  psTemp + 2 * VECSZ, 1);
  /* triplicate */

ccopy(VECSZ,
  psTemp + VECSZ - shift, 1,
  psTemp, 1);
  /* rotated spectrum */

cvfftb(psTemp,
  psTemp,
  VECSZ,
  -1); /* time series */
```

```
fftInvRanging =
  vsip_ccfftip_create_f(
    (vsip_length) VECSZ,
    1.0 / (float) VECSZ,
    VSIP_FFT_INV,
    0,
    VSIP_ALG_TIME);
vsip_cvcopy_f_f(pcvSample,
  vsip_cvputoffset_f(pcvSampxDup,
  2 * VECSZ)); /* triplicate */

vsip_cvcopy_f_f(
  vsip_cvputoffset_f(pcvSampxDup,
    VECSZ - shift),
  vsip_cvputlength_f(pcvCenterdx,
    VECSZ));
  /* rotated spectrum */

vsip_ccfftip_f(fftInvRanging,
  pcvCenterdx); /* time series */
```

Vector Memory Allocation Before And After

```
if ((psMainSpec
     = (complex *)valloc(
       sizeof(complex) * FFTSIZE))
  == NULL)
  printf("Error\n"), fflush(stdout);
else
  vclr((float *)&psMainSpec->cr),
    1,
    sizeof(complex) * FFTSIZE);
```

```
if ((pcvMainSpec
     = vsip_cvcreate_f(FFTSIZE,
       VSIP_MEM_NONE))
  == NULL)
  logMsg("Error\n",0,0,0,0,0,0);
else
  vsip_cvfill_f(
    vsip_cmplx_f(0.0, 0.0),
      pcvMainSpec);
```

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Surprises And Subtleties

- FIR Filter Inversion And Ramp-Up
  - VSIPL Version More Flexible
  - VSIPL Optionally Preserves Filter State From Previous Batch
  - Impossible To Obtain Identical Behavior Porting From Sky Math Library
- Inverse FFT Scaling
  - Behavior Built-In To Sky Math Library
  - Optional In VSIPL
  - Obvious In Hindsight / Devilish To Spot

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More Minor Subtleties

- vsdiv() Maps To vsip_svmul_f() With Reciprocal Of Scalar
- cvexp() Maps To vsip_veuler_f()
- VSIPL Clipping Mechanism More General Than SML
  - Requires Analysis To Obtain Equivalent Behavior

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Implementation Costs

- 2.5 Man Months Expended
  - Inception To Delivery (4 Calendar Months)
  - Includes Learning Curve
  - Sky Computers Customer Service And Algorithms Group Very Supportive Of This Effort
- SLOC Growth Nominally 10%
- Execution Time Penalty 15%
  - Misleading To Discuss As Percentage
  - Actually A Fixed Overhead
  - Higher Frequency Applications Will See Larger Penalty As Percentage Of Execution Time

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Target Platform Constraints

- FIR Filter Decimation Moved To Hardware (GC214 DDR)
  - Input Complex Time Series Presented At Slightly Later Point In Signal Processing Algorithm
  - Significant Execution Time Relief
  - EchoTek Provided Support For This Transition
- MPI VSI/Pro Product Update Overlapped Application Migration
  - Mutually Beneficial Issue Resolution Cycle With MPI Customer Service
    - Function Inventory
    - Numeric Precision
    - Compiler Switches
    - Address Relocation
    - Library Footprint
  - VSI/Pro 1.10 Is A Solid Product

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Steps To Port In Place To Target Platform

1) Compile Source In New Target Development Environment
   - Link With New Vendor Library
   - Identify And Resolve Unimplemented VSIPL Function Issues
   - Identify And Resolve Input / Output Issues Peculiar To New Target Environment (vxWorks)
   - Protect Platform Specific I/O With Conditional Compilation Switches

2) Test And Verify Numeric Results
   - Correct Errors
   - Iterate Until Accurate
   - Likely To Succeed On Initial Iteration

3) Deliver

- Numeric Errors (If Any) Anticipated To Be Precision Issues

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Subtleties And Implementation Costs

- Minor Subtlety
  - Little Known taskSpawn() Argument VX_ALTIVEC_TASK Required
  - Opaque Error "Altivec Unavailable" Provided By BSP If Flag Is Omitted
- Implementation Costs
  - 2 Man Weeks Expended
  - 4 Calendar Months, Due To External Impacts Not Part Of This Effort
  - Execution Time Benefit: Application Cycles 4 Times As Fast, But FIR Filter Is No Longer In Software

Benefits

- Migration Was Unmitigated Success
- Application Now Excellent Example Of "Write Once / Run Anywhere" Goal Espoused On VSIPL Website
- SEASPARROW Program Can Legitimately Distribute Algorithm Enhancement Costs Across Larger Installed Platform Population

Observations On VSIPL

- Extremely Useful And Well Documented Standard
- "Development Mode" Deserves More Rigorous Specification
  - Rather Crash And Examine Stack Trace Than Exit Gracefully And Not Know What Happened
- Numerical Accuracy / Precision Is Ambiguous
  - Result Precision Or Calculation Precision
  - Possible To Obtain Numerically Different Results From Conforming Implementations Through Vendor Interpretation Of This Point
- Test Suite Fidelity Still Emerging

Observations On Migration

- Effort Is Bounded
  - No Dead Ends, No Meandering
  - Atmosphere Of "Turning The Crank" During Migration
- Low Risk
  - Application Will Still Function When Effort Concludes
- Future Maintenance Easier To Staff
  - Availability Of VSIPL Literate Software Engineers Independent Of Vendor-Specific Signal Processing Library
- Enthusiastically Recommend Similar Efforts

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