Partitioning of a Signal Detection Algorithm to a Heterogeneous Multicomputing Platform

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Abstract:

This paper explores the tradeoffs involved in mapping a signals intelligence algorithm to general-purpose processor and field programmable gate array (FPGA) based technology. Specifically, a prototypical signal detection algorithm is described. This algorithm consists of an Fourier transform based frequency channelizer followed by a statistical signal detector.

The system examined consists of a single 14-bit real-valued input stream sampled at 100 MSa/s. With a Fourier transform overlap factor of 75%, this results in a total sustained bandwidth of 1 GB/s. The bandwidth is too large for a single commercial off-the-shelf (COTS) processor to get on and off board, leading to systems solutions using multiple processors.

The multiple-processor partitioning problem is looked at from both the time and frequency domains. For the example application, the strengths and weaknesses of each strategy are examined. The influence of the choice of processing platform on the partitioning affects the final solution as well. General-purpose processors typically run at very high speeds, but perform only a small number of operations per clock cycle. FPGAs, on the other hand, can perform thousands of operations per clock cycle, but operate with a slower clock frequency. These differences, as well as other system features such as the interprocessor communication subsystem, dramatically affect the viability of potential partitioning solutions.

It is shown that successful multiprocessor partitioning depends on the entire system. Of critical importance are the features and performance of the processing nodes and the interprocessor communications system. When the requirements are greater than a single aspect of the system can handle, this paper explores the possibility of utilizing excess capacity in other areas of the system to balance the system loading. Finally, some of the issues that arise from extending the system to multiple antenna streams are also explored.

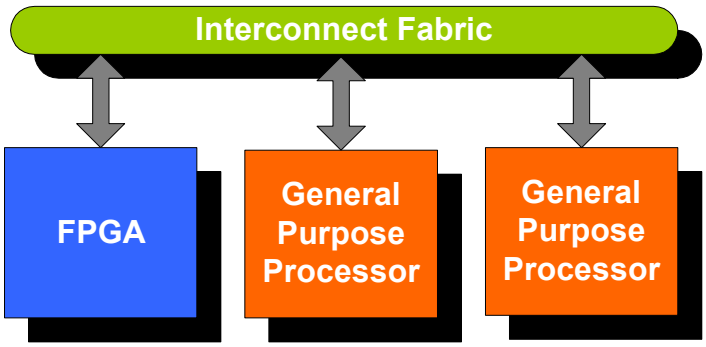

Figure 1: An example heterogeneous multicomputing computing platform.

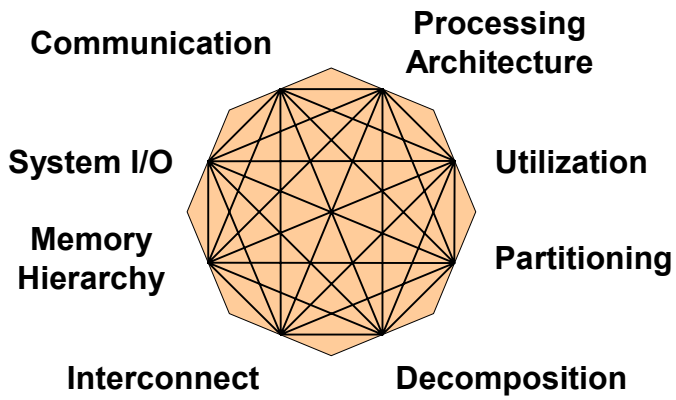

Figure 2: Some of the issues associated with heterogeneous multicomputing applications.