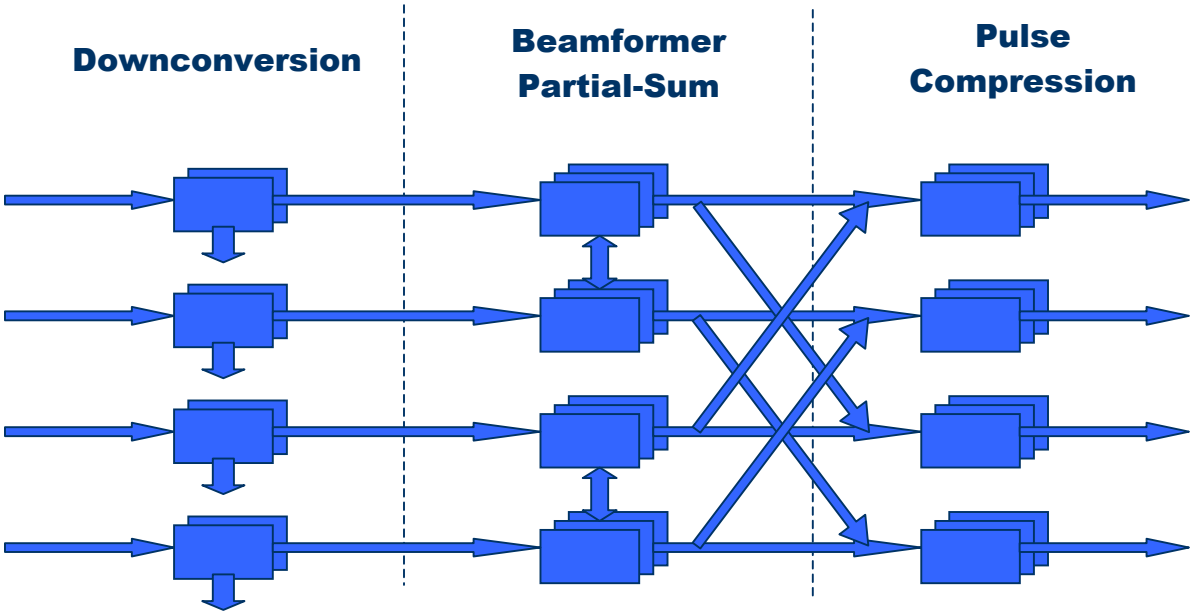
Beamforming for Radar Systems on COTS Heterogeneous Computing Platforms

Mr. Jeffrey Rudin
Mercury Computer Systems, Inc.
Phone: (978) 967-1686
Fax: (978) 256-8596
Email: jrudin@mc.com

Abstract:
The introduction of high-speed analog-to-digital converters has resulted in many of the traditional front-end and sub-array combining functions of multi-function, phased-array radar systems being performed in the digital rather than in the analog domain. Due to the intense amount of processing that is required, many of these functions had to be realized in hardware. This was originally accomplished using VLSI ASICs. However, the advent of multi-million gate field-programmable gate array (FPGA) has permitted these complex digital processing functions to be put in small packages with a degree of design flexibility that is normally associated only with software. This permits more of the radar functions to be realized in commercial off-the-shelf (COTS) hardware by obviating the need of full-custom VLSI in many cases.

The incorporation of FPGA technology into COTS processing subsystems permits more complex designs to be created than could be achieved by general-purpose or digital signal processors alone. Simply incorporating FPGAs into single board computers could solve many signal processing problems. However, because of the complexity of the signal processing in a multi-function radar system, a distributed, parallel-processing architecture is usually required. In addition, the trend toward an increasing number of input channels and the formation of a greater number of simultaneous beams requires a high degree of interconnection among the processing elements. Therefore, the technology used to interconnect the computing elements must be flexible enough to accommodate different architectures and system requirements. Furthermore, the interconnection technology should be scalable enough to enable early design prototyping as well as system deployment over a wide range of mission platforms.



Example Interconnection of Radar Front-End Processing

This paper focuses on the impact of using a heterogeneous distributed computing system for digital beamforming in a multi-function radar system. The interconnection of FPGAs requires balancing the utilization of FPGA resources for endpoint logic I/O with that for processing requirements. A balance must also be struck in the mapping of functions between the FPGAs and the programmable processors in a heterogeneous system. Very frequently, the scaling of particular requirements will require the interconnection topology to change rather than just scale. We examine several different sets of requirements and the subsequent mapping to the heterogeneous computing platforms and the tradeoffs involved. Particular focus is given to the changes in functional allocation and the resulting system topologies.