An Ultra-High Performance Architecture for Embedded Defense Signal and Image Processing Applications

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Abstract:

This briefing describes the development of a novel, ultra-high performance next-generation Single-Instruction/Multiple-Data (SIMD) processing architecture originally designed to realize immersive, photo-realistic 3-D simulations. This low-power, Multi-Threaded Array Processor (MTAP) architecture provides for hundreds and ultimately thousands of processing elements, each with optional floating point hardware, to perform data parallel processing on image and signal processing applications as well as for compression, encryption, search, and general sensor processing applications. The technology is supported by a flexible development environment, including assembly language and C-based language support, as well as a cycle accurate simulator, with plans to develop industry standard API Libraries based upon VSIPL and, ultimately, HPEC-SI. This new technology, being developed by World*Scape* and ClearSpeed, has been shown to provide ten to one hundred times the overall performance of PowerPC or Pentium-based architectures, especially when performing image and signal processing functions, such as FFTs or filters. In general, the architecture has been shown to provide significant throughput, size, and power advantages for embedded processing applications.

ClearSpeed Technology Limited is developing the MTAP architecture that provides a scalable array of Processing Elements (PEs) on a single die. Currently 64 and 256 PE devices are planned, although the array can scale to 1,000s of PEs. The technology is complemented by a scalable packet switched bus architecture called ClearConnect that has been designed to support the high bandwidths required for many applications. The technology is proven in silicon and is capable of delivering per device peak performance of over 100 GFLOPS while dissipating less than 5 Watts. The processor is supported by a professional Software Development Kit (SDK) and includes an optimizing C compiler, graphical debugger and a full suite of supporting tools and libraries.

World*Scape* Defense Company has been developing key algorithms and library functions such as FFTs and FIR filters which efficiently utilize the architecture and floating point per PE hardware to gain exceptional performance at very low power dissipation levels. Specific application work, supported by the Office of Naval Research, has been undertaken for radar processing with raw throughput numbers for functions such as FFTs, complex multiplies, filters, etc. significantly higher than other industry standard processing and DSP platforms. This briefing also describes new levels of benchmark performance for FFT per second per watt that provide the basis of plans for embedded SAR processing systems on small UAV's. High level C and VSIPL library support are planned and currently under development.

Lockheed Martin Naval and Electronic Surveillance Systems has been trained in the use of the SDK, and has ported some key, high-performance application benchmarks, such as radar pulse compression, for performance comparison with general purpose processing architectures. Results have shown the potential for considerable performance enhancement for airborne, shipboard, ground-based and undersea tactical signal and image processing systems.

In this briefing, we describe an embedded processing architecture that promises a performance advantage over conventional general-purpose processors of one or two orders of magnitude. Finally, the results of a DoD benchmark algorithm run on the cycle-accurate simulator in summer, 2003, will be presented and compared with general- purpose processor performance.