

Development of an FPGA-Based Two-Transform Pulse Compressor

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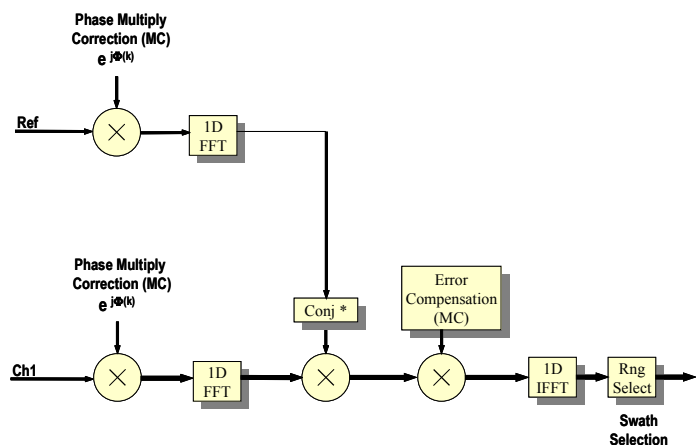
Case Study Examples of High Performance Embedded Computing
Advanced Digital Front-End Processors

Abstract:

Recent advances in Field Programmable Gate Array (FPGA) technologies have resulted in high gate count and high performance FPGA parts which offer a cost-effective and short development cycle solution for computation intensive signal processor applications. These parts provide an attractive middle ground between Commercial Off-the-Shelf (COTS) boards employing Digital Signal Processor (DSP) chips with relatively low computational element densities, and expensive and long lead time custom Application Specific Integrated Circuit (ASIC) designs. COTS FPGA boards and core development software are available through a variety of vendors which allow FPGA solutions to be developed on custom signal processing applications with efficient use of resources and a short design and development cycle time.

Fixed point vs floating point processing cores were investigated as part of the design tradeoff, using MATLAB simulations to create performance predictions and verifying the predictions using actual core designs to process test vectors. As part of the design process different bit width data paths were considered for the fixed point core designs in order to tradeoff core sizes versus precision required for the algorithm implementation. As a rule of thumb, a 5:1 size reduction is obtained using fixed point processing cores as opposed to full floating point cores. For this particular pulse compressor design, fixed point cores were chosen to help minimize the hardware size.

Using the flexibility of this programmable technology, a high-bandwidth two-transform pulse compressor is implemented using Fast Fourier Transforms (FFTs) in an FPGA board architecture. This processor is targeted at processing complex data streams of over 500 MHz utilizing long FFT lengths of up to 64K. The architecture is modular in design, allowing a parallel processing architecture in order to achieve high throughputs via the use of multiple round-robin processing nodes, as well as multiple channel processing. For a single channel consisting of a received signal and a reference waveform signal (REF) which are to be cross correlated and pulse compressed using a two transform frequency domain approach, the throughput is estimated to be 160 billion operations per



second (GOPS). This single channel design is implemented on two standard size full-length PCI cards. Several parallel channels may be implemented to achieve effective throughputs of several trillion operations per second (Tera-ops). Results of this study will be presented, including actual throughputs versus predicted.

To demonstrate viability of this approach, Annapolis Wildstar IITM PCI boards are used to create a COTS solution requiring virtually no hardware development, allowing the focus to be on algorithms and data flow considerations. The pulse compressor architecture includes high-speed (800MB/sec) data busses as an integral part of the design, facilitating inter-board communication and avoiding data path bottlenecks. The Annapolis CoreFireTM core development environment allows fast and efficient prototyping of the design without requiring the use of VHDL code development for complex cores such as the large FFTs.

