Kernel Benchmarks and Metrics for Polymorphous Computer Architectures

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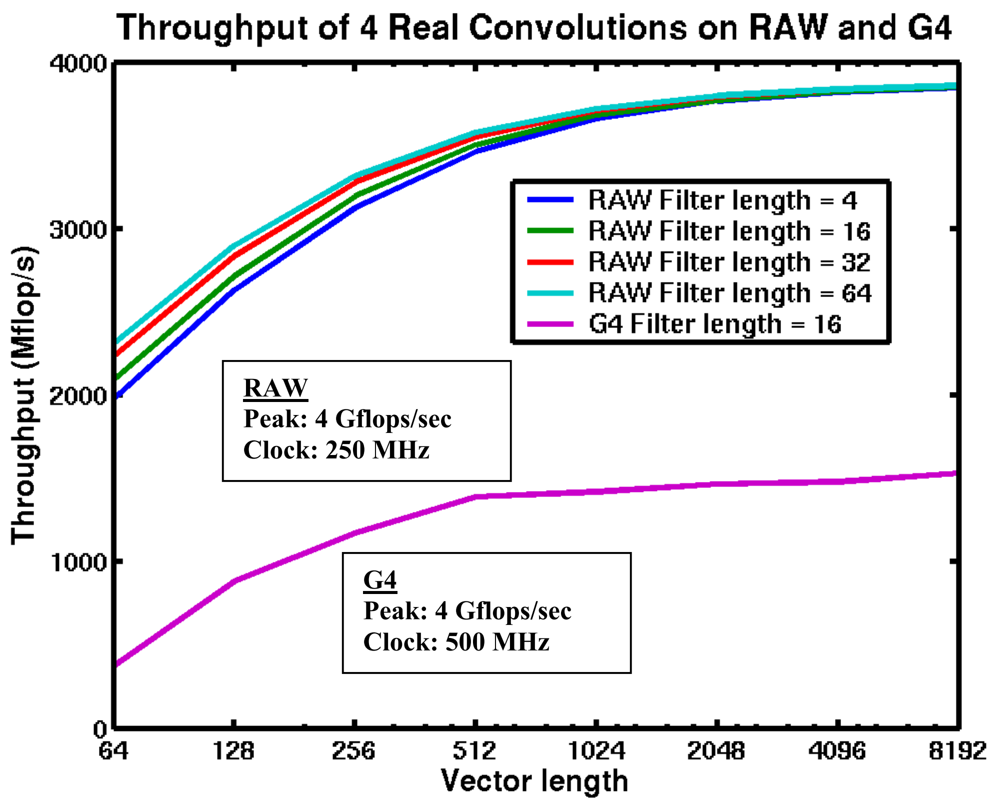
Polymorphous computer architectures (PCA) are new computer architectures being developed under a DARPA/IPTO program to support mission agility for future high performance DoD embedded applications. These new architectures will have the ability to "morph" into different modes of execution with the goal of delivering uniform, high performance across a large variety of different processing types and workload compositions. Examples of these architectures include the MIT RAW machine [5], the Stanford Smart memories project [3], and the University of Texas TRIPS machine [4].

To evaluate the applicability of PCA to next generation ISR (intelligence, surveillance, reconnaissance) applications, MIT Lincoln Laboratory has developed example applications and kernel benchmarks that span the space of embedded ISR application requirements. Matlab code for an example ISR application, with elements of feature-aided tracking [6], is being analyzed by teams developing PCA architectures. In addition, seven kernel benchmarks that represent important pieces of this application have been defined. These seven kernels are FIR filter, singular value decomposition, constant false-alarm rate (CFAR) detection, corner turn, pattern matching, graph optimization via genetic algorithm, and database search.

An important first step in evaluating PCA architectures is the implementation of these kernel benchmarks on processors used in modern embedded applications. This implementation provides a baseline for future comparisons. MIT/LL has implemented these seven kernels on the PowerPC G4 processor. The results show that the throughput varies considerably from kernel to kernel. This variation in performance is reflected in a metric known as *stability*. Defined by Kuck [2], stability is the ratio of the minimum to the maximum throughput for a particular set of problems. A chief benefit of PCA architectures is expected to be their stable performance across a range of kernels and data sizes.

Hoffman [1] has implemented convolution and many other kernels on the RAW simulator using scalable systolic algorithms. Hoffmann's throughput results for real convolution on a simulated 250 MHz RAW are shown in Figure 1 and compared with a similar kernel on a 500 MHz G4. Both machines have a peak throughput rated at 4 Gflops/sec. Clearly, the simulation results show that RAW has the potential to perform much better than the G4 on this kernel.

In this talk, we present and analyze performance results for several PCA kernels on the MIT RAW simulator and on a RAW test board. We compare these with the baseline performance results obtained on the PowerPC G4 in terms of throughput, stability, efficiency and power efficiency.



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