High Performance Embedded Computing Software Initiative (HPEC-SI)

Jeremy Kepner* (kepner@ll.mit.edu) MIT Lincoln Laboratory, Lexington, MA 02420

Abstract

The High Performance Embedded Computing Software Initiative (see www.hpec-si.org) is addressing the military need to advance the state of embedded software development tools, libraries, and methodologies to retain the nation's military technology advantage in increasingly software-based systems. Key accomplishment include completion of the first demonstration and the development of the Parallel VSIPL++ standard. Currently the HPEC-SI effort is on track towards its goal of changing the state-of-the-practice in programming DoD HPEC SIP systems.

1 Introduction

The High Performance Embedded Computing Software Initiative (HPEC-SI) involves a partnership of industry, academia, and government organizations to foster software technology insertion demonstrations, to advance the development of existing standards, and to promote a unified computation/communication embedded software standard. The goal of the initiative is software portability: to enable "write-once/run-anywhere/run-anysize" for applications of high performance embedded computing (see [7, 4, 10, 8, 9, 18, 12]).

This paper gives a brief overview of the HPEC-SI program objectives, technical objectives and program plans. Detailed progress of the demonstration, development and applied research activities that are taking place within the HPEC-SI can be found in the HPEC2002[15, 20, 27], GOMAC2002[26, 5, 11, 21, 23], GOMAC2003[28, 6, 14, 17, 22], and other conferences[16, 13].

*This work is sponsored by the High Performance Computing Modernization Office, under Air Force Contract F19628-00-C-0002. Opinions, interpretations, conclusions and recommendations are those of the author and are not necessarily endorsed by the United States Government.

2 Program Objectives

HPEC-SI is organized around demonstrations, standards development and applied research. Each of these activities is overseen by a Working Group. The demonstrations team Prime contractors with FFRDC or academic partners to use currently defined standards, evaluate their performance, and report on how well their needs are being met. The first demonstration was with the Common Imagery Processor (CIP) and successfully showed the use of MPI communication standard ([1]) and the VSIPL computation standard ([2]) to achieve portability (while preserving performance) across shared servers and distributed memory embedded systems. The Development Working Group is extending the VSIPL standard to include parallel object-oriented software practices already prototyped by the research community. This effort is tightly coupled with military demonstrations, and provides the next generation of standards with direct feedback from the military user base. The Applied Research Working Group is also taking a longer term view to assess the potential impact of a variety of emerging technologies such as: fault tolerance and dynamic scheduling, self-optimization, and next generation high productivity languages.

3 Technical Objectives

The HPEC-SI program uses three principal metrics to measure the progress of its efforts:

- Portability (reduction in lines-of-code to change port/scale to new system);
- Productivity (reduction in overall lines-of-code);
- Performance (computation and communication benchmarks).

Traditionally, it has always been possible to improve in two of the above areas while sacrificing the third. HPEC-SI aims to improve quantitatively in all three areas.

HPEC-SI expects to achieve at least a 3x reduction in the number code changes necessary to port an application across computing platforms. This improvement will primarily be achieved through the use and enhancement of open software standards (MPI and VSIPL) that will insulate applications from the details of the underlying hardware. An equivalent reduction in code changes will also be seen when porting from one size of platform to another. This will be achieved by the development of a unified computation and computation standard (Parallel VSIPL) which will allow applications to be moved from a computer with N processors to a computer with M processors with minimal code changes.

HPEC-SI expects to achieve a 3x reduction in the total number of lines of code necessary to implement an application. This productivity improvement will be primarily be through the use of higher level object oriented languages (e.g. C++) as well as a unified computation and communication library which will abstract away many of code intensive details of writing a parallel program.

HPEC-SI expects to achieve a 1.5x increase in performance over existing approaches on some computation and communication benchmarks. This is primarily due to an increased level of abstraction which allows the increased use of "early binding" in the application, in the library and in the compiler. [Early binding is the process of building data structures in advance that increase performance at runtime.]

4 Summary

The current achievements of HPEC-SI include the successful utilization of the Vector Signal and Image Processing Library (VSIPL) and the Message Passing Interface to demonstrate a tactical synthetic aperture radar (SAR) code running without modifications and at high performance on parallel embedded, server and cluster systems. HPEC-SI is also creating the first parallel object oriented computation standard by adding these extensions to the VSIPL standard. The parallel VSIPL++ standard will allow high performance parallel signal and image processing applications to take advantage of the increased productivity offered by object oriented program as well as the performance advantages found using advanced expression template technology. The draft object oriented specification and reference code are both available on the HPEC-SI website and are being tested by a variety of early adopters. Finally, HPEC-SI is evaluating advanced software technologies such as fault tolerance and the use of higher level languages to determine which aspects are ready for future standardization. Combined, all of these efforts are successfully changing the state-of-the-practice in programming DoD HPEC SIP systems. Critical to this effort has been the availability of a wide variety of HPCMO systems (Mercury, Sky, SGI, Compaq, IBM, Linux, andFPGA) that has allowed the testing and demonstration of advanced software technologies for DoD signal and image processing applications.

References

[1] Message Passing Interface (MPI), http://www.mpi-forum.org/

[2] Vector, Signal, Image Processing Library http://www.vsipl.org/

[3] High Performance Embedded Computing Software Initiative http://www.hpec-si.org/

[4] E. Baranoski, High Performance Embedded Computing Software Initiative (HPEC-SI), DoD HPCMO Signal/Image Processing Forum (SIP 2001), May 15, 2001, Biloxi, MS

[5] D. Campbell and M. Richards, Object Oriented Extensions to the Vector, Signal, and Image Processing Library (VSIPL) standard, DoD HPCMO Signal/Image Processing Forum (SIP 2002/GOMAC 2002), Mar 13, 2002, Monterey, CA

[6] D. Campbell C++ and parallelism extensions to the VSIPL standard, GOMACTECH 2003, Apr 4, 2003, Tampa, FL

[7] C. Holland, Keynote Address, High Performance Embedded Computing Workshop (HPEC 2001), Sep. 25, 2001, Lexington, MA

[8] C. Holland, The Convergence of HPC and HPEC, Panel at Supercomputing 2001, Nov. 13, Denver, CO

[9] J. Grosh, Invited Talk: A DoD Perspective on High Performance Computing, High Performance Embedded Computing Workshop (HPEC 2001), Nov. 27, 2001, Lexington, MA

[10] J. Kepner, Defining Future High Performance Embedded Computing Software, DoD HPCMO Signal/Image Processing Forum (SIP 2001), May 15, 2001, Biloxi, MS

[11] J. Kepner, High Performance Embedded Computing Software Initiative (HPEC-SI), DoD HPCMO Signal/Image Processing Forum (SIP 2002/GOMAC 2002), Mar 13, 2002, Monterey, CA

[12] J. Kepner, DoD Sensor Processing: Applications and Supporting Software Technology, Supercomputing 2002, Baltimore, MD, Nov 2002.

[13] J. Kepner, High Performance Embedded Computing Software Initiative (HPEC-SI), HPCMO User's Group Conference, Jun 10 2003, Bellevue, WA

[14] J. Kepner, High Performance Embedded Computing Software Initiative (HPEC-SI), GOMACTECH 2003, Apr 4, 2003, Tampa, FL

[15] M. Mitchell and J. Oldham, VSIPL++: Intuitive Programming Using C++ Templates HPEC 2002, Sep 2002, Lexington, MA

[16] M. Mitchell and J. Oldham, Parallel VSIPL using VSIPL++, Supercomputing 2002, Baltimore, MD, Nov 2002.

[17] M. Mitchell and J. Oldham, VSIPL++: Intuitive Programming Using C++ Templates GOMACTECH 2003, Apr 4, 2003, Tampa, FL

[18] Maj Gen P. Nielsen, Keynote Address: Perspective on Embedded Computing HPEC 2002 Workshop, Lexington, MA, Sep 2002

[19] E. Rutledge and J. Kepner, PVL An Object Oriented Software Library for Parallel Signal Processing, Cluster 2001, October 9, 2001, Newport Beach, CA

[20] M. Richards et al, Development Status of the Vector, Signal, and Image Processing Library (VSIPL), HPEC 2002 Workshop, Lexington, MA, Sep 2002

[21] T. Skjellum and G. Bourdreaux, Early Binding and C++ for VSIPL and VSIPL++, DoD HPCMO Signal/Image Processing Forum (SIP 2002/GOMAC 2002), Mar 13, 2002, Monterey, CA

[22] T. Skjellum and G. Bourdreaux, Early Binding and C++ for VSIPL and VSIPL++, GOMACTECH 2003, Apr 4, 2003, Tampa, FL

[23] H. Spaanenburg, Virtualization, DoD HPCMO Signal/Image Processing Forum (SIP 2002/GOMAC 2002), Mar 13, 2002, Monterey, CA

[24] B. Sroka, Standards-Based Real-Time Embedded High Performance Computing: Common Imagery Processor, DoD HPCMO Signal/Image Processing Forum (SIP 2001), May 15, 2001, Biloxi, MS

[25] B. Sroka and D. Szakovits, Standards-Based Real-Time Embedded High Performance Computing: Common Imagery Processor, High Performance Embedded Computing Workshop (HPEC 2001), Nov. 29, 2001, Lexington, MA

[26] B. Sroka, Standards-Based Real-Time Embedded High Performance Computing: Common Imagery Processor, DoD HPCMO Signal/Image Processing Forum (SIP 2002/GOMAC 2002), Mar 13, 2002, Monterey, CA

[27] B. Sroka and D. Szakovits, Standards-Based Real-Time Embedded High Performance Computing: Common Imagery Processor, HPEC 2002, Sep 2002, Lexington, MA

[28] B. Sroka, Standards-Based Real-Time Embedded High Performance Computing: Common Imagery Processor, GOMACTECH 2003, Apr 4, 2003, Tampa, FL