The Decomposition of HPEC Applications Mapped to The Natural Decomposition of a Solution Architectures – Another Way to Think About Solving HPEC Problems

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Abstract: In the HPEC historical past, all large-scale computer architectures that were designed, developed, and delivered by the so-called DSP vendors generally were of the "kitchen sink" design approach. Each board unit basically incorporated all of the features that one could possibly want into a single unified design. Processors, I/O, memory, and interconnects were built in whether they were needed or not. They were all available in a single unified product thereby increasing per slot functionality but many times at the burden of complexity, reliability, and overall cost of ownership. While this was convenient and appropriate at the time, the user was required to procure and support all of the key building blocks with solutions that were, for the most part, vendor unique and quite frankly not always necessary for application success.

Through the examination of high performance, high end embedded computing applications, it can be shown that nearly all of them have a very distinctive and natural decomposition of the problem space such that there lies a distinct I/O and data management portion and another distinct compute portion. Wrapped around both components is the need for global (infrastructure wide) communications as well as system state and health management. We further learned that in most instances that the delivered solution was burdened with many facilities that were simply not of any value and in many cases robbed the system of valuable real estate and/or reliability simplicities.

The onslaught of blade servers has caught the eye of many a developer with the *apparent* low cost of ownership, but upon close examination, they too suffer from feature bloat for most HPEC applications. However; the shear simplicity and ease of use in small form factor blade servers are attractive for many needs that don't *really* require harsh, dense packaging but not in the real time Signal and Image Processing arenas that High Performance Embedded Computers are warranted. Right form factor, right price, wrong feature set for HPEC needs.

This paper will address an industry unique architectural approach to addressing the needs of HPEC applications through the use of distinctive, upgradeable, and naturally decomposed solution elements. This approach provides an application space with the freedom to address complex solutions needs without the burden of the "kitchen sink" approach. The focus of this talk is on the adoption of highly flexible Data Acquisition Servers and highly focused Compute Servers, each of which addresses the unique and very demanding needed of real time signal and image processing. Advances in COTS components (hardware and software) are cornerstones of this capability and future flexibility.

A comparison between the more traditional HPEC systems and the Next Generation Architectures will be presented for key applications within both the Defense and Commercial communities.