High Performance Embedded Computing Workshop at MIT/LL
(23-25 September 2003)

1. Title: Hybrid Optical/Digital Processor for Radar Imaging

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4. Presentation session:

Presentation does not need to be limited to the US Only session.

5. Presentation format:

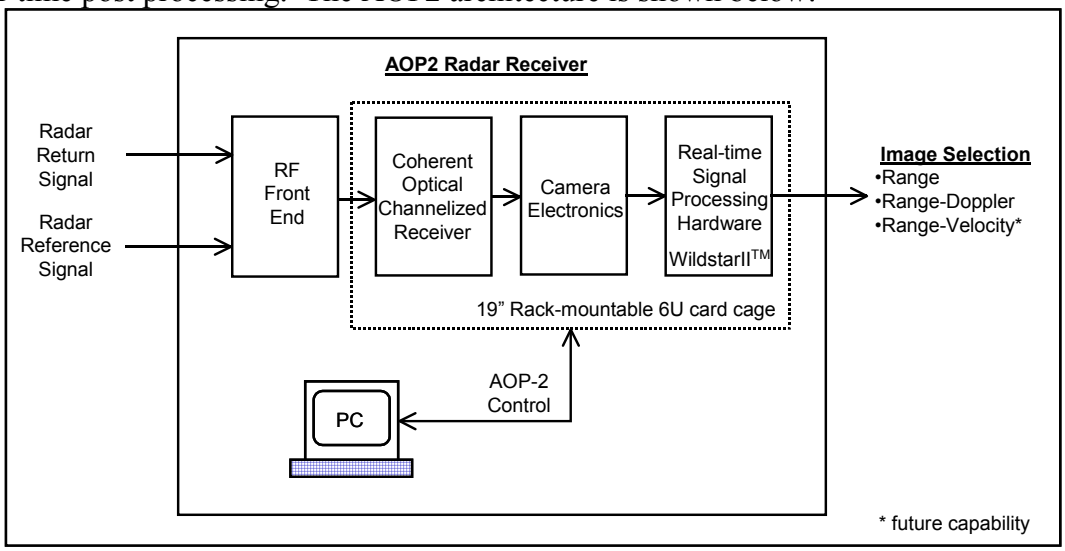
Authors prefer an oral presentation.

6. Areas of work addressed:

a. Embedded Computing for Global Sensors and Information Dominance
b. Advanced Digital Front-End Processors
c. Automated Tools for Embedded System Development

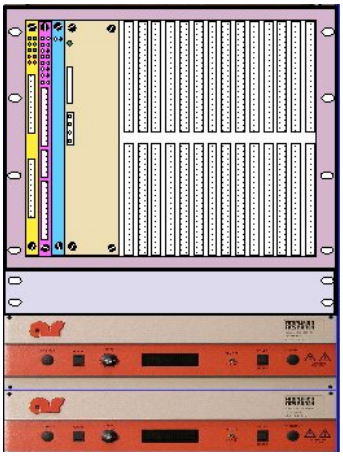
7. Abstract

Essex is developing a prototype hybrid optical/digital processor for radar image formation using wideband arbitrary waveforms. The processor is called the Advanced Optical Processor (AOP) and is a hybrid acousto-optic/digital processor that generates high dynamic range, range-Doppler images from wideband radar returns. This work is being funded by the Missile Defense Agency's office of Manufacturability and Producibility (MDA/MP) and will be tested at the MIT/LL Lexington Development Facility. The processor supports high resolution processing necessary for target discrimination and kill assessment by enabling the use of true arbitrary, wideband waveforms. The selected architecture combines the advantages of both embedded optical signal processing for the front-end receiver and embedded high-speed digital signal processing for the real-time post processing. This combination provides the capacity to process signals with 1 GHz of instantaneous bandwidth in a real-time environment without the need for wideband analog-to-digital converters (ADCs). This is achieved in a compact lightweight package that combines both an optical coherent channelizer and a WILDSTARII™ FPGA VME board from Annapolis Micro Systems that performs the real-time post processing. The AOP2 architecture is shown below:



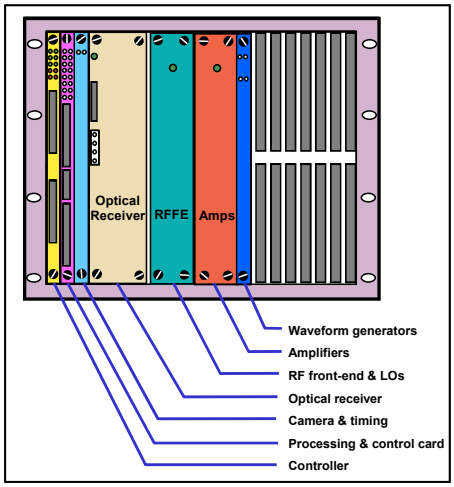
AOP2 Architecture

The AOP2 prototype hardware is shown below:



AOP2 Prototype Hardware

The production hardware can easily fit into a single 6U card cage, as shown below, without significant development costs.



AOP Production Configuration

By removing complex software and custom digital hardware, the cost for this processor is significantly less than an "all-digital" solution, even in modest quantities. The cost effectiveness of this processor allows use at the sub-array level for desired operational flexibility and performance enhancements, such as beamforming and STAP.

The development of this processor has been accelerated with the use of the AMS CoreFire™ FPGA Application Builder. This tool has allowed the mapping of the post processing algorithms to the COTS AMS FPGA hardware with minimal effort. Selected AOP2 algorithms were running as a demonstration in the WildstarII™ for the AOP2 critical design review with just a few weeks of effort. CoreFire™ also provided a hardware-in-the-loop debugger that allowed us to insert test data into the designs in the FPGAs and then review the test vectors from the host as they ran through each part of the algorithm. The AMS hardware configuration is a 6U form factor with 3 Xilinx Virtex II™ 6000 series FPGAs. This WILDSTARII board also has two I/O daughter card positions providing in excess of 4 GB/s I/O bandwidth. The DSP algorithms running in this hardware include:

1. data formatting algorithms
2. calibration algorithms
3. range-compression algorithm
4. Doppler compression algorithm
5. data storage formatting
6. display formatting
7. system timing and control functions

The chosen hardware can perform these algorithms in real-time and is flexible such that changes in the algorithms are easily accommodated. There is no operating system required so integration issues with a single board VME control computer are minimal.

Presented in this paper will be the architecture description and integration of the optical and FPGA technologies, along with updated test results.