Delivered Performance Predictions and Trends for RISC Processors in Radar Applications

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Topic Area:
Performance Modeling and Simulation for Benchmarking Embedded Systems
Case Study Examples of High Performance Embedded Computing
Algorithm Mapping to High Performance Architectures

Abstract: Deployed radar and signal intelligence (SIGINT) systems require enormous amounts of real-time computational capability that must adhere to very confined power, weight and volume budgets. Computational requirements have been increasing as advanced adaptive signal processing techniques make their way from laboratories to deployed platforms. In many cases the computational requirements are increasing while power, weight and volume budgets are increasing only marginally if at all. These conflicting trends show an increase in processing requirements within existing platforms are driving physical and environmental budgets to ever higher levels of efficiency from commercial off-the-shelf (COTS) processing systems. This paper will address current trends in COTS processor designs and explore models that hopefully will predict how well these processors should perform per watt/kg/m^3. The models will focus on space-time adaptive processing (STAP) and SIGINT processing requirements and how they map to very large-scale arrays of general-purpose programmable processors.

System designers are currently examining various technology options for increasing the levels of sustainable performance per watt/kg/m^3 for their applications. These options include field-programmable gate arrays (FPGAs), alternative RISC processor architectures, and even a possible return to digital signal processor (DSP) devices. Each of these device classes has an associated cost of programmability, flexibility, upgradability, and interoperability with other devices. The question of efficiency of the device is not so easily stated, though, and is a function of the processing algorithms that must be performed as well as how well the devices can be interconnected in a large parallel processing system. It does not appear to be a question any more of "will" a particular device be applicable in high-end deployed systems, but "where" is it of the highest value in a processing chain. Heterogeneous systems are a certainty in future system designs. Part of these heterogeneous systems will continue to be large-scale processing arrays of advanced RISC processors that still hold much value for large amounts of the emerging application requirements. This presentation will examine trends in extracting more performance out of advanced RISC processors in order to meet stringent platform environmental and power budgets.

Although the most flexible and easiest to program, extracting performance out of a RISC-type processor is a challenging endeavor. Today's processors are highly complex and sophisticated architectures that include RISC cores, vector processing units, multi-stage memory hierarchies as well as high levels of integration of I/O interfaces and advanced data transport facilities. Furthermore, to use these devices in practical applications continues to require building large arrays of these devices in complex highly interconnected configurations. A system wide understanding of these complex systems is required in order to model their performance in radar and SIGINT applications. The models will include the effects of concurrent accesses of local memory systems by both the processor and network. System-level relative performance levels of existing and future RISC processors by various vendors will be examined, as will the effects of interconnect technologies and the network interface devices.