VSIPL for Diverse Architectures (Pentium 4 to DSPs)

Mr. Brian Chase
Mr. WenhaoWu
Dr. Anthony Skjellum
MPI Software Technology, Inc
Phone: (662) 320-4300, ext. 13
Fax: (662) 320-4301
E-mail: brian@mpi-softtech.com
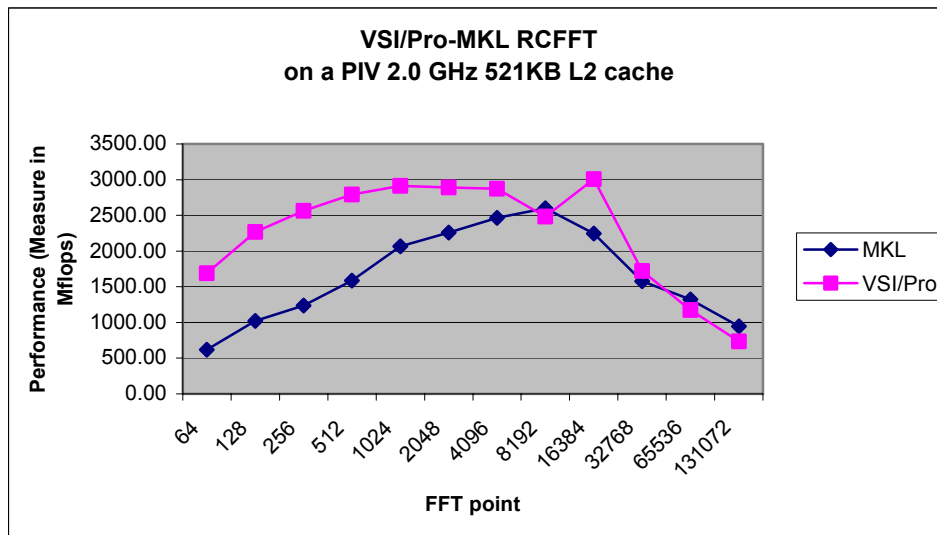E-mail: wenhao@mpi-softtech.com
E-mail: tony@mpi-softtech.com

Many companies have described their experiences with using Motorola G4 processors to provide the VSIPL CoreLite standard for military and medical computing, and others have described their efforts with highly optimized Core and Core+ profiles.

This poster uses the experience of MPI Software Technology's existing Core+ optimized VSIPL implementation for G4 as the springboard for supporting other platforms of emerging interest to COTS, defense, medical and imaging customers.

Three kinds of technologies are occurring in military computing that may unseat the preeminence of low-power G4-style RISC processors: 1) The growing power of DSPs including better development environments, as typified by TI TMS320C6x family (as opposed to SHARC 2106x, which was harder to program strictly from C and libraries), 2) The use of medium-power systems with Pentium 4 based blades, 3) The growing perception that PowerPC is lagging Pentium in overall performance

Furthermore, the clock speed of Intel Pentium line of processors is now reaching three or more GHz. Also, the vector processing registers (SSE) available on the Pentium III or later provide several orders of improved performance for single precision floating point operations. Additionally, the well-known Pentium family provides a cost-effective COTS solution for embedded hardware designers as well as the end users. This means that although high power consumption, their Flops/Watt are becoming more attractive.

MPI Software Technology now has a fully optimized VSIPL (Core and CoreLite) library, known as VSI/Pro, for Pentium 4 / SSE platform targeting Linux, Windows, and VxWorks operating systems. The FFT performance of VSI/Pro is consistently better than Intel's Math Kernel Library (a.k.a MKL), as illustrated in the following graph. VSI/Pro has a carefully designed API, i.e., VSIPL, which is well fitted to the needs of the signal and image processing community in the defense and medical industries.

VSI/Pro-MKL RCFFT
on a PIV 2.0 GHz 521KB L2 cache

Performance (Measure in Mflops)

3500.00
3000.00
2500.00
2000.00
1500.00
1000.00
500.00
0.00

64 128 256 512 1024 2048 4096 8192 16384 32768 65536 131072

FFT point

◆ MKL
■ VSI/Pro

The Texas Instrument's TMS320C67 family of processors is a general purpose DSP chip that is specifically designed for FFT and FIR operations. This family of processor is widely used and accepted by the signal processing community with the applications including software radio, modems, and sonar. Unique features of this family of processor include: 1) a very deep pipeline and 2) a very large instruction word (VLIW) architecture. Texas Instruments provides an integrated development environment known as Code Composer, which supports the C and C++ programming languages. Also, Tiny C Compiler has the ability to produce correct code for this DSP chip. The porting of VSI/Pro to this family of processor has started by the hand tuning of FFT operations and the algorithm mapping from the original RISC/CISC implementation to DSP chip.

Experiences, results, plans and future work for supporting Intel Pentium 4 and Texas Instruments TMS320C67 family within VSI/Pro are described in this poster.