Optimizing System Compute and Bandwidth Density for Deployed HPEC Applications

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Abstract: Many high-end deployed military and commercial applications share a common need to achieve high to very high compute and bandwidth density in the smallest possible volume. In addition, deployed military applications layer on additional environmental requirements such as higher levels of shock, vibration, endurance vibration, temperature, and condensing humidity. Each of those adds constraints on the solution space for maximizing compute and communication density.

Not all HPEC applications can use the same solution due to varying limits on total size or weight and varying levels of ruggedness. For example, the size and weight requirements differ greatly for manned surveillance aircraft, large UAVs, and small UAVs. This presentation will explore different options for high-density system designs while meeting the requirements for each of these applications.

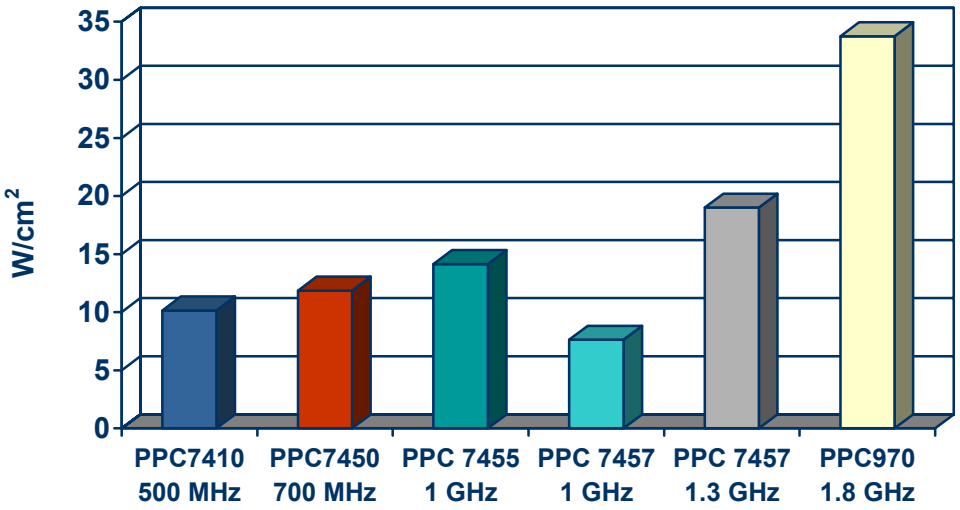

Figure 1. Power flux of recent and near-term PowerPC processors.

A big obstacle is the well-known trend of increasing power consumption for newer faster processors. Faster processors require faster memory, faster interconnect, and more I/O. Not as well known is the power increase due to the move to high-speed switch fabrics clocked up to multiple GHz and memory systems being clocked well into the hundreds of MHz. A high-speed switch fabric and memory system exacerbate the thermal problem even as it solves bandwidth problems. In these cases, it is the large number of components and the concentrated point sources of power that create the biggest challenge beyond that of the overall increasing power and shrinking die size. This combines with the increasing power consumption to create a significant challenge. Figure 1 shows a comparison of past and present processor power flux.

Yet these are not the only demanding components in the system. FPGAs, SRAM, on-board power supply FETs, integrated DC/DC converters, and various ASICs must all be examined as point sources of heat in today's designs. Previous designs have 70% or more of the power in the system going to the processors alone. For current designs, it is typically 40-50%, with the balance going to areas such as interconnect, memory, and supporting components. Large FPGAs used for computing can consume 20W, and the power supply FETs can have the power flux (W/cm^2) of a similar magnitude to the processors.

When component package type is taken into account (e.g., plastic TSOP for DDR-DRAM, PBGA for ASICs), the other components mentioned can approach the same power and thermal management challenge as the processor. Designing a system to optimize the performance density with respect to each of these is challenging.

For any given selection of processor, fabric, and support chips, the areas of system design that can be worked to maximize overall power density, and therefore performance density, are largely driven by the mechanical aspects of the board form factor and the resulting cooling methods for the boards and chassis.

Traditionally, the choices for cooling methods have been convection-cooled (air-cooled) and conduction-cooled. Recent years have seen a growing interest in spray-cooling (evaporation-cooled), because it offers a greater potential for thermal dissipation than either air-cooled or conduction-cooled while providing the benefits of a sealed enclosure for environments with little air, dirt, or corrosive elements. Yet when the size, weight, and maturity of the various cooling methods are examined, air-cooling is shown to meet the right set of tradeoffs against the commercial and military requirements for much of the HPEC space.

This presentation will describe one technique for extracting greater thermal efficiency from an air-cooled design we call "finely managed air." In this approach – covers on the boards, heat-sinks captive in these covers, and airflow shaping in the covers, slots, and chassis inlet areas – are all designed together as a system to carefully direct all available air flow over the hottest components to extract the maximum thermal efficiency. While in conventional board and heat sink design the majority of the air wants to flow around the high-impedance heat sinks instead of through them, the new approach uses features in the cover that directs air through the heat sinks. Since high velocity flow tends to ride up the backplane and starve the front of the board, there is also a need to balance the airflow front to back within a slot to also maximize cooling efficiency.

Features built into the cover achieve this in a way to have the minimum effect on overall pressure drip.

Such "finely-managed air" designs have been verified using both Computational Fluid Dynamics (CFD) modeling and lab measurements of operational hardware at the component, board, and system level, and this paper will present the analysis of that data. In addition to the airflow-shaping aspects of the cover, the cover also adds a very important ruggedizing structural element to the board while not penalizing the available surface area of the PWB with stiffeners, mounting holes, and keep-out regions.

To further maximize the effect of such an approach, each processor or high-power component should get an independent flow of air. Currently high-end deployed commercial off-the-shelf (COTS) high-density designs use large area boards, such as VME 9U x 400mm, to maximize the number of processors per given volume using both the available height and depth. New commercial form factors have similar approaches, such as PICMG3.0 with an 8U high board and less deep at 280mm. In those tall-board designs, components not on the inlet edge of the board will see air that was already heated by processors or other high-power components lower on the board. There can be as many as three to six rows of high-power components in an attempt to maximize processing physically in the layout.

In the face of these thermal considerations, concurrent engineering must be given to board and chassis design. The optimal location for high-power components is along the bottom of the board on the leading edge of the airflow. A long, shorter board therefore provides the maximum thermal dissipation for a system by combining this longer leading edge with a lower flow resistance due to the shorter nature of the board. In order to get the highest density in a given vertical space, two boards stacked vertically with an air intake in the middle provide a significant improvement over past practice in the thermal dissipation capacity for a given board set. An example of such a configuration is shown in Figure 2. For both boards, the hottest components are placed on the leading edge of the airflow.

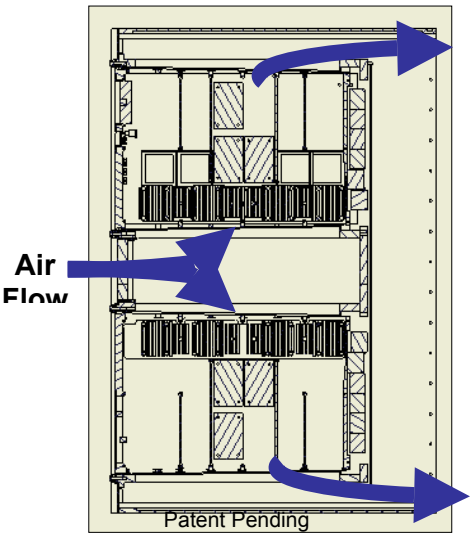

Figure 2. Two short boards mounted vertically sharing the same air intake to minimize vertical space.

This organization allows for continued use of a large common backplane. A large common backplane remains the linchpin to achieving tens of GB/s of inter-chassis bandwidth in a very compact and very high-speed signaling environment.

This presentation will discuss such design trade-offs for different deployed HPEC environments in terms of size, power, and weight constraints.