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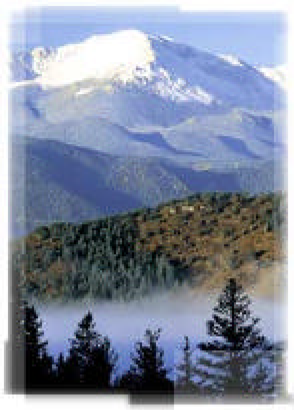

A Comparison of Two Computational Technologies for Digital Pulse Compression

Presented by Michael J. Bonato
Vice President of Engineering
Catalina Research Inc. – A Paravant Company

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Goals of Presentation

- Highlight major design trade-offs when comparing an ASIC and FPGA solution for pulse compression
- Provide information to help choose the right tool for the right job

Outline

- Overview of pulse compression
- Comparison of computational approaches
- Trade-offs when mapping algorithm to an ASIC or FPGA
- Example analysis
- Other considerations
- Summary

Pulse Compression Overview

- Convolves return signal with complex conjugate of transmit waveform
- Produces peak where correlation occurs [1]
  - Indicates location of target in range
  - Compressed pulse narrower than width of transmit waveform (higher range resolution)
  - Helps radar obtain good ranging accuracy with low instantaneous transmitter power
- Ability to produce narrow peaks depends upon transmit waveform's
  - Bandwidth
  - Duration (length)
- Bandwidth • duration = Time Bandwidth Product (TBP)
- Higher TBP [2]
  - Finer range resolution
  - Lower instantaneous transmitting power
  - Requires more computational horsepower

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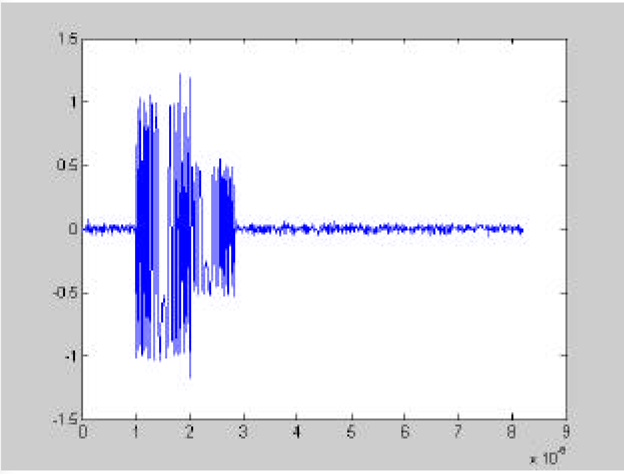
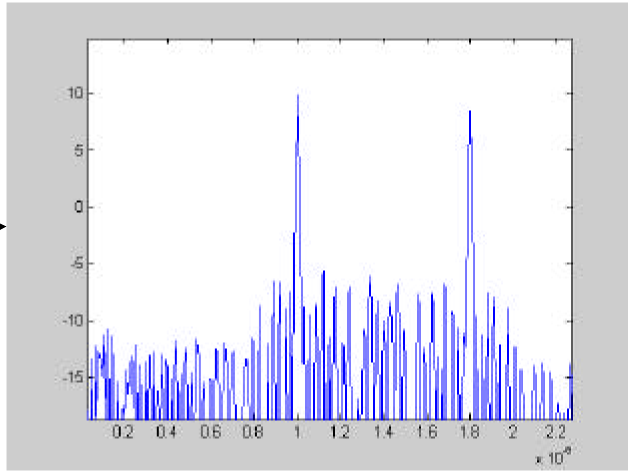
Pulse Compression Illustration



Received Signal (t)

Pulse Compression

(convolution with complex conjugate of transmit waveform)



Compressed Received Signal (t)

- Two targets in receive window hard to pinpoint in time (range)
- Targets clearly stand out after compression

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Approaches to Digital Pulse Compression

- Time domain convolution
  - Filter time samples of receive window using Finite Impulse Response (FIR) filter
  - Use transmit waveform samples as tap values (number of taps = TBP)
- Frequency domain complex multiplication
  - FFT (of receive window)
  - Complex multiplication by complex conjugate of FFT (transmit waveform)
  - IFFT
  - Overlap by TBP if sectioned convolution*
- Both approaches mathematically equivalent
  - Convolution (time) ⇔ multiplication (frequency)

** For DSP implementation, TBP = duration • sampling rate*

Which Approach to Use?

- Computational efficiency is the driving factor
- Operations defined here as total number of multiplies and adds
- Number of FIR operations per input sample:

  $= 8N - 2$ *where* $N =$ *number of taps*
- Number of FFT operations per input vector:

  $= 5\, N \log_2 N$ *where* $N =$ *FFT length*
- Both equations assume complex data

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Example: TBP = 256

FIR operations = 8 * 256 - 2 = 2046

→ 2046 operations need to happen every new input sample

FFT operations:

→ assume an FFT length of twice the TBP

$5 * 512 * \log_2 (512) = 23{,}040$

→ this needs to happen twice (once for FFT, once for IFFT)*

= 2 * 23,040 = 46,080 operations

→ i.e. for every input vector, 46,080 operations need to occur

→ assuming sectioned convolution, overlap input vectors by TBP

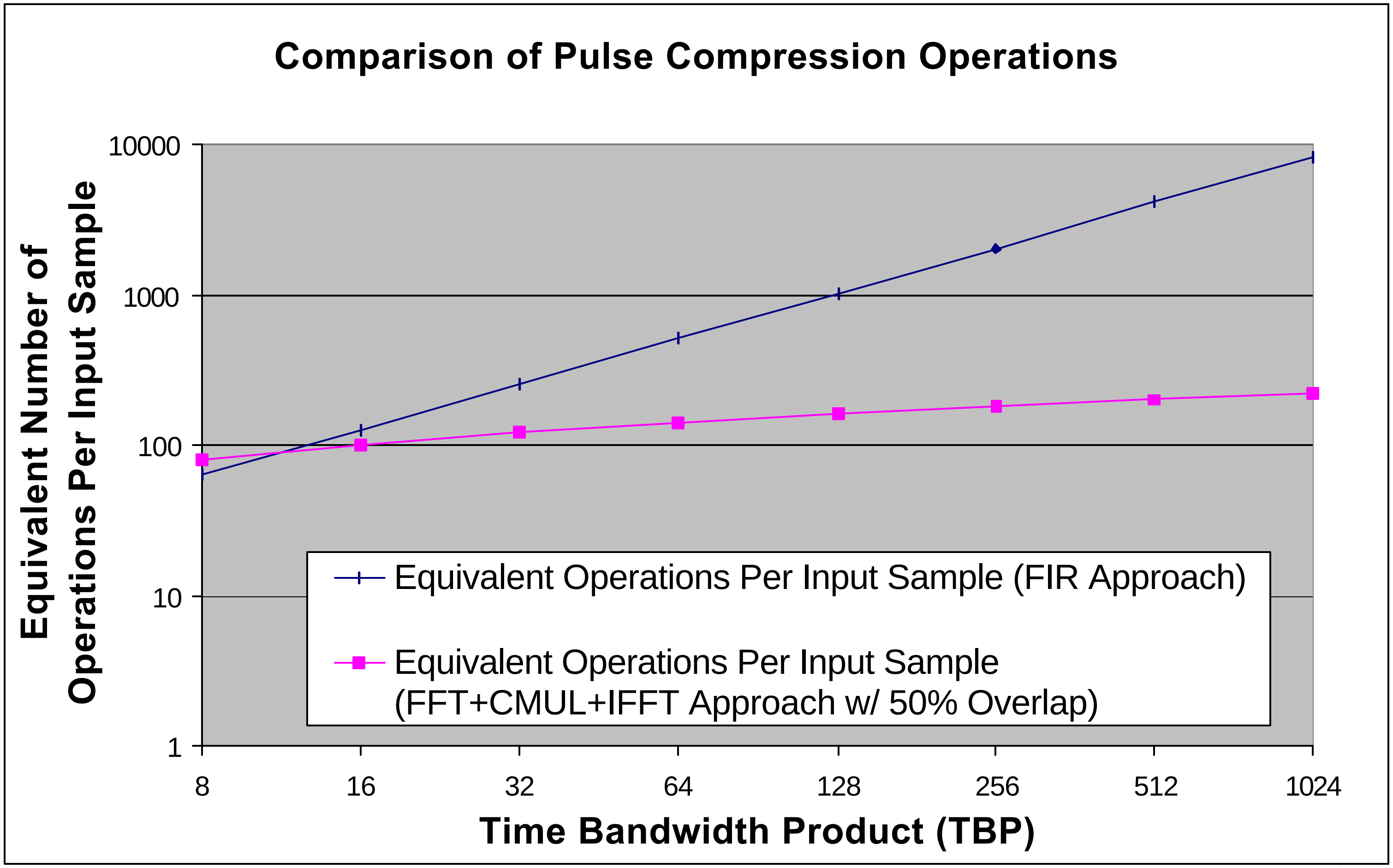
→ thus, effective operations per input sample:

46,080 / (512 – 256) = 180 operations per new input sample

FFT approach is over 11 times as efficient as FIR in this case!

* *Time domain window can be folded into first pass of FFT*
Complex multiplication can be folded in with first pass of IFFT

Computational Efficiency of FFT vs. FIR



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Mapping FFTs into Hardware

- ASIC or FPGA?
  - ASIC: Pathfinder-2 programmable frequency domain vector processor
  - FPGA: Xilinx VirtexE
- Trade space considerations:
  - Radar system parameters
    - TBP
    - Number of samples in the receive window
  - Number of bits (precision and dynamic range)
  - Performance (measured in Pulse Repetition Frequency)

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Radar System Parameters

- FFT size determined by ($TBP + N_s - 1$) [3]
  - TBP = number of samples representing transmit pulse
  - N_s = number of samples in receive window

    $= [\ P_w + 2\ (R_w / c)\ ] \cdot F_s$

    P_w = *pulse width of transmit waveform*
    R_w = *range window of the radar*
    c = *speed of light*
    F_s = *sampling rate of digital receiver system*

- Longer FFTs need more
  - Processing
    - Larger radix cores
    - More passes through the data
  - Memory
  - Bits

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Number of Bits

- Today’s high speed ADCs
  - 14 bits up to 100 MSPS
  - 12 bits up to 200 MSPS
- FFT radix computations create word growth
  - Radix 2 can cause growth of one bit just due to additions
  - Radix 4: two bits
  - Radix 16: four bits
- Longer FFT lengths require more radix passes
  - More opportunity for growth

Floating Point vs. Fixed Point [4]

- Floating point
  - Can lead to truncation or rounding errors for both addition and multiplication
  - Overflows highly unlikely due to very large dynamic range
  - Requires more hardware resources than fixed point (adders in particular)
- Fixed point
  - Truncation or rounding errors occur only for multiplication
  - Addition can lead to overflows
    - Avoid by making word length sufficiently long (may not be practical)
    - Avoid by shifting (scaling), but this can compromise precision

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Performance: Pulse Repetition Frequency

- Defines how often the radar transmits pulses
- Higher PRFs imply
  - Faster update rates and track loop closure
  - Lower Doppler ambiguity
  - Higher range ambiguity
- Time between transmit pulses sets a limit on the processing time available
- Conversely, the processing time required for a given FFT size limits the achievable PRF

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Example Analysis

- Assume the following radar system parameters:

Transmit Pulse Width	10.2 usec
A/D Sampling Rate (Baseband)	10 MSPS
Range Window	10 Km

Calculate FFT Size

- TBP = pulse width • sampling rate
  - 10.2 usec • 10 MSPS = 102 samples
- N_s (number of samples in the receive window)
  - [10.2 usec + 2 (10 Km / c)] • 10 MSPS = 769 samples
- FFT size = 102 + 769 – 1 = 870 samples minimum
- Round to power of two: 1024 points
- Well within capabilities of Pathfinder-2 or FPGA

Define Word Length

- Assume 14 bit ADC
- Assume one bit growth per radix 2 stage (ten stages for 1K FFT)
- Implies word length of 24 bits for fixed point operations
  - For worst case input to FFT
  - Assuming rest of system can support the dynamic range
- Fixed point implementation must
  - Define sufficiently large word (accumulator), or
  - Scale data input to each radix stage
    - Blindly shift at every iteration (Xilinx 1K FFT 16 bit core) [5]
    - Implement “intelligent” shifting (e.g. block floating point)
- Not an issue for floating point (Pathfinder-2)

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Processing Performance

- Algorithm: window → CFFT → CMUL → IFFT for 1K vector
- Pathfinder-2
  - 35.4 usec at 133 MHz clock
  - Achievable PRF = 1 / 35.4 usec = 28.3 KHz assuming one channel
  - 32 bit IEEE floating point
- Xilinx XCV2000E sizing estimate
  - Assume 80 MHz clock rate
  - Achievable PRF (with 75% utilization) ≈ 15 KHz (one channel)
  - 24 bit fixed point
    - Overflow still a concern
    - 24 bits would suffice for 1K FFT alone (most applications)
    - Does not provide for growth due to IFFT
    - Scaling / shifting logic will still be needed

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Additional Design Considerations

- Part count
  - Minimum Pathfinder-2 solution requires
    - Pathfinder-2 ASIC
    - Three external address generators
    - Three SRAM banks
    - Small FPGA to act as a controller
  - Entire solution could fit in XCV2000E
- Parts costs (estimated)
  - Pathfinder-2 solution = $1,500
  - Xilinx XCV2000E = $2,900
- Design flexibility and development
  - What if you decide to change FFT sizes?
  - What if you want to match against multiple transmit waveforms?

Summary

- Less demanding pulse compression application good match for FPGAs
- More demanding system requirements quickly drive solution towards a Pathfinder-2 type of approach

Pulse Compression Application (1K Vector Size)	
Pathfinder-2 (ASIC)	XCV2000E (FPGA)
Higher PRFs	Lower PRFs
Higher Parts Count	Lower Parts Count
Less Expensive	More Expensive
Minimal Precision and Dynamic Range Concerns	Valid Dynamic Range and Precision Concerns
Easily Scalable to More Demanding Algorithms	Not Easily Scalable to More Demanding Algorithms

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[1] Cook, Charles E., "Pulse Compression – Key to More Efficient Radar Transmission," *Barton Radar Systems Volume III*, 1960.

[2] Skolnik, Merrill I., *Introduction to Radar Systems*, McGraw-Hill Book Co., NY, 1962.

[3] Brigham, Oran E., *The Fast Fourier Transform*, Prentice-Hall Inc., Englewood Cliffs, NJ, 1974.

[4] Rabiner, L. R. and Gold, B., *Theory and Application of Digital Signal Processing*, Prentice-Hall Inc., Englewood Cliffs, NJ, 1975.

[5] Xilinx Product Specification., "High Performance 1024-Point Complex FFT/IFFT V1.0.5," Xilinx Inc., 2000.

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