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Systems Integration

Multidimensional Performance Modeling for Advanced Embedded Signal Processors

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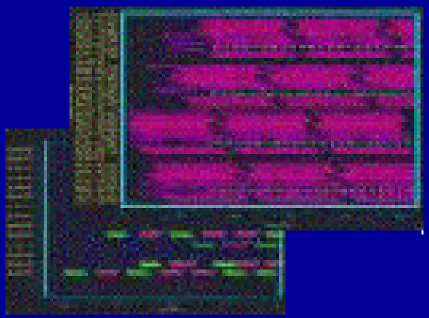
Multidimensional Performance Modeling

DoD missions/systems require new approaches/ tools to exploit emerging reconfigurable technologies to form polymorphous/power aware systems.

- **Problem:**
  - — **Traditional performance modeling approaches \are unable to address emerging requirements and component technologies. This is a result of an increased awareness and need for dynamically adaptive or reconfigurable systems, particularly in the area of power dissipation/performance.**

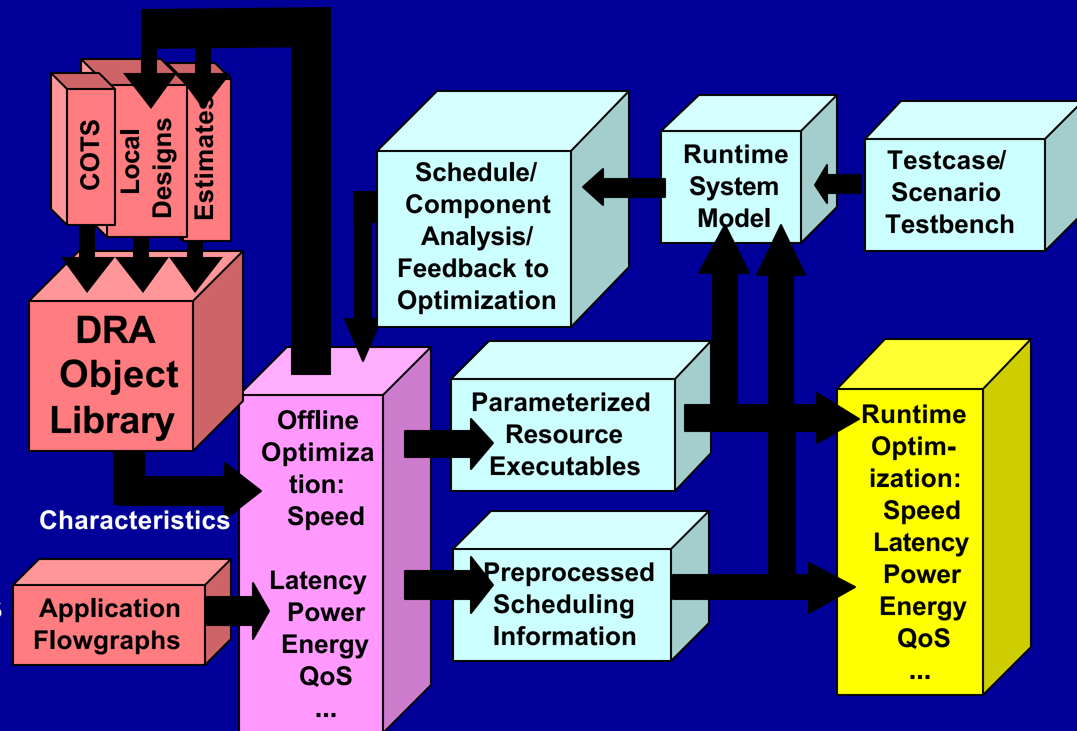
- **Goal(s)/Objectives(s)**
  - — **Define methods/algorithms to acurately model and optimize reconfigurable architectures and functions (services) required to support multidimensional performance modeling.**
  - — **Apply ideas developed from InfoPad, ACS, PAC/C, DARES, PCA, and MSP to develop a uniqe new rapid prototyping/optimization capability.**



- **Approach**
  - — **Define features required to support accurate performance and multidimensional modeling and optimization of DRAs.**
  - — **Evaluate algorithms/methods for performing intelligent, reactive dynamic scheduling.**
  - — **Evaluate algorithms/methods for performing offline analysis, data reduction, pattern recognition, and execution planning.**

Dynamically Reconfigurable Architectures

A Methodology for Verifiable, Validatable Polymorphic Architectures

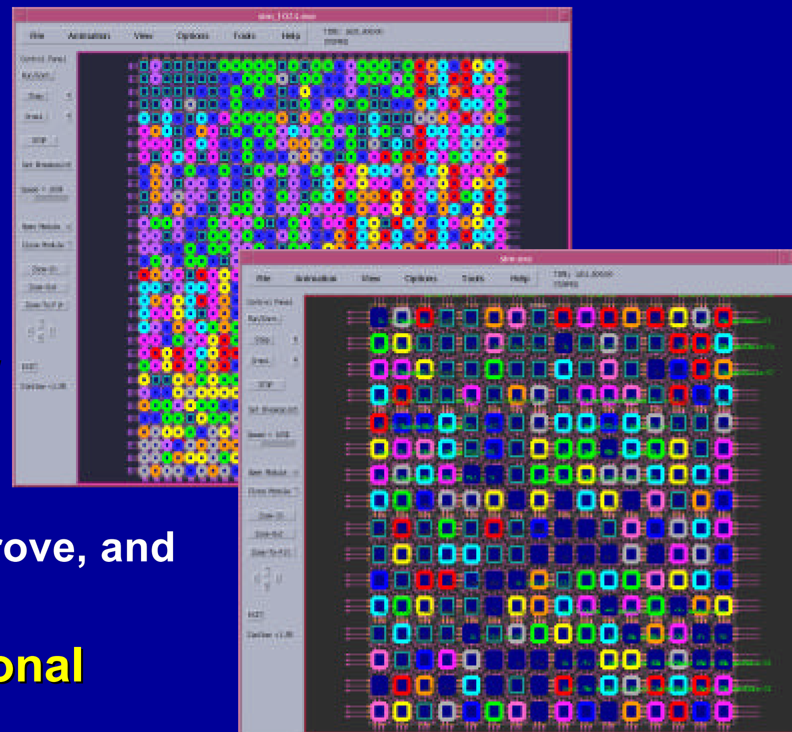


DRA Optimization Process Flow

- Based upon a two phase optimization process - offline and online
- Offline optimization
  - — Overall goal: perform component selection, pruning, data extraction and sensitivity analysis that will maximize the effectiveness of the online optimization
  - — Selects an optimum set of verified, validated components from existing libraries
  - — Facilitates analysis to identify potential implementations more optimal to the application
  - — Identifies dependencies/relationships in the data flow graph that will facilitate online scheduling
- Online optimization
  - — Components are selected for execution at runtime based upon dynamic figures of merit
  - — Figures of merit are complex functions of component characteristics

Key Aspects of Approach

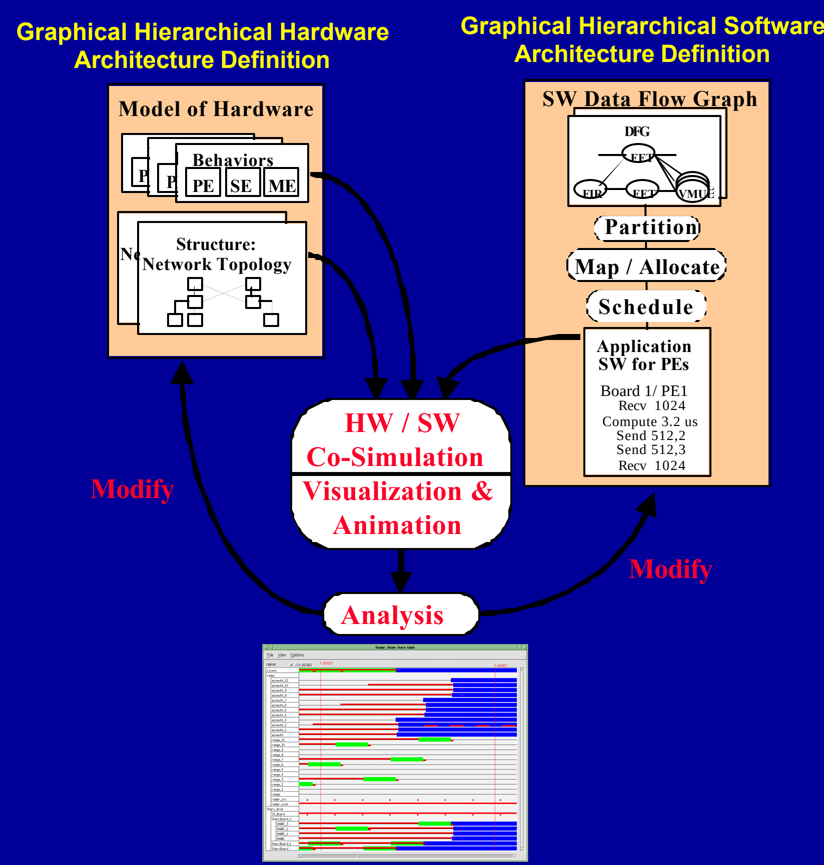
- **Dealing with overwhelming flexibility**
  — Management of complexity and methods of abstraction/simplification
- **Two stage optimization**
  — Offline (component and subsystem) and online (scheduling)
- **Methodology for generating/optimizing/ representing components and reconfigurable devices**
  — Develop operating points, analyze, improve, and abstract



- **Dynamic scheduling with multidimensional goals/constraints**
  — “Toolkit” approach using offline extracted information
- **Offline information extraction and optimization of scheduling**
  — Analysis/characterization/abstraction of tasks/graphs
- **Constraint/goal simplification using modes**
  — Abstraction method minimizing computation and enforcing interfaces
- **Reuse of existing capability to perform the required analysis and data visualization**
  — Use the internally developed CSIM

CSIM — HW/SW Virtual Prototyping Capabilities and Features

- **CSIM has demonstrated the ability to model complex signal processor network behavior and performance**
- **CSIM is a C-based, hierarchical simulation environment for modeling system, subsystem, and individual module/component HW/SW performance**
- **CSIM's independent use of HW/SW models provides a path for reducing development costs as well as the life cycle costs**
- **CSIM provides a common environment for developing and verifying system, subsystem, and module HW/SW interfaces**

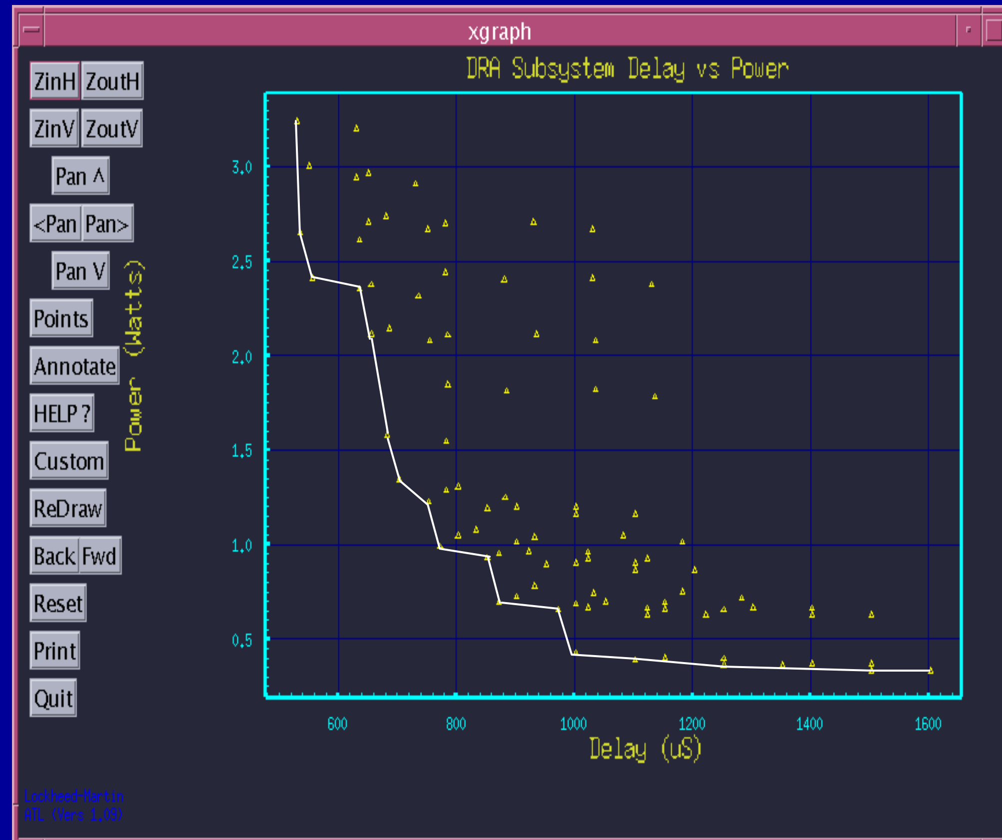


Produces Animated and Static Simulation Timeline Displays as well as processor, communication, and memory statistical data

Detailed information on CSIM can be found at: www.atl.lmco.com/proj/csim/

Automated Support to Offline Analysis/ Optimization

- **Each task/component (i.e. fft, fir) is abstracted by several parameters (i.e. throughput, latency, power, size, etc.)**
- **Each task may have several differently optimized implementations**
- **An online library of implementations is selected**
- **The application(s) of interest are simulated using a subset of the available components**

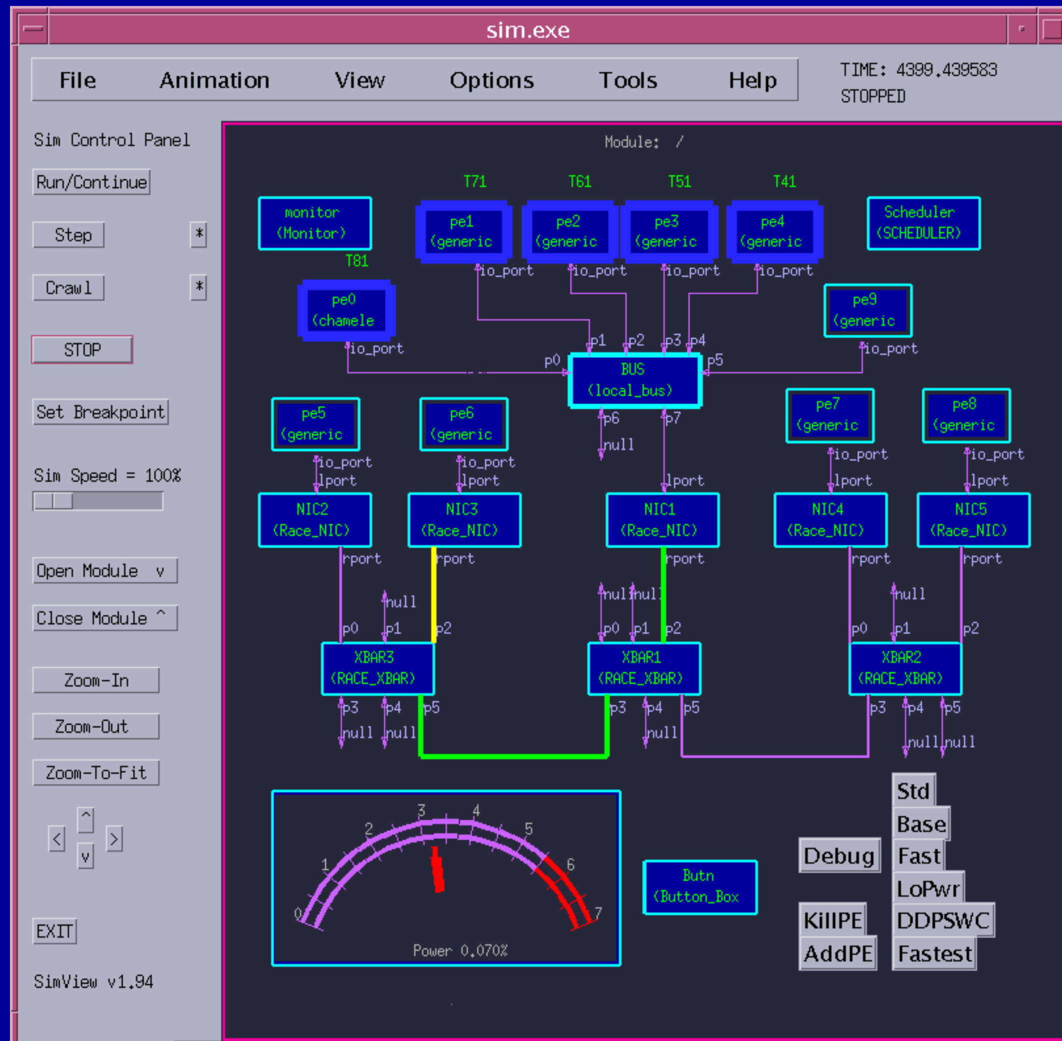


Design space resulting from evaluating a representative signal processing application

- **The results of simulating each subset is characterized with respect to the parameters of interest**
- **The characterizations are used to identify a subset of implementations that are most optimal across the parameters of interest**

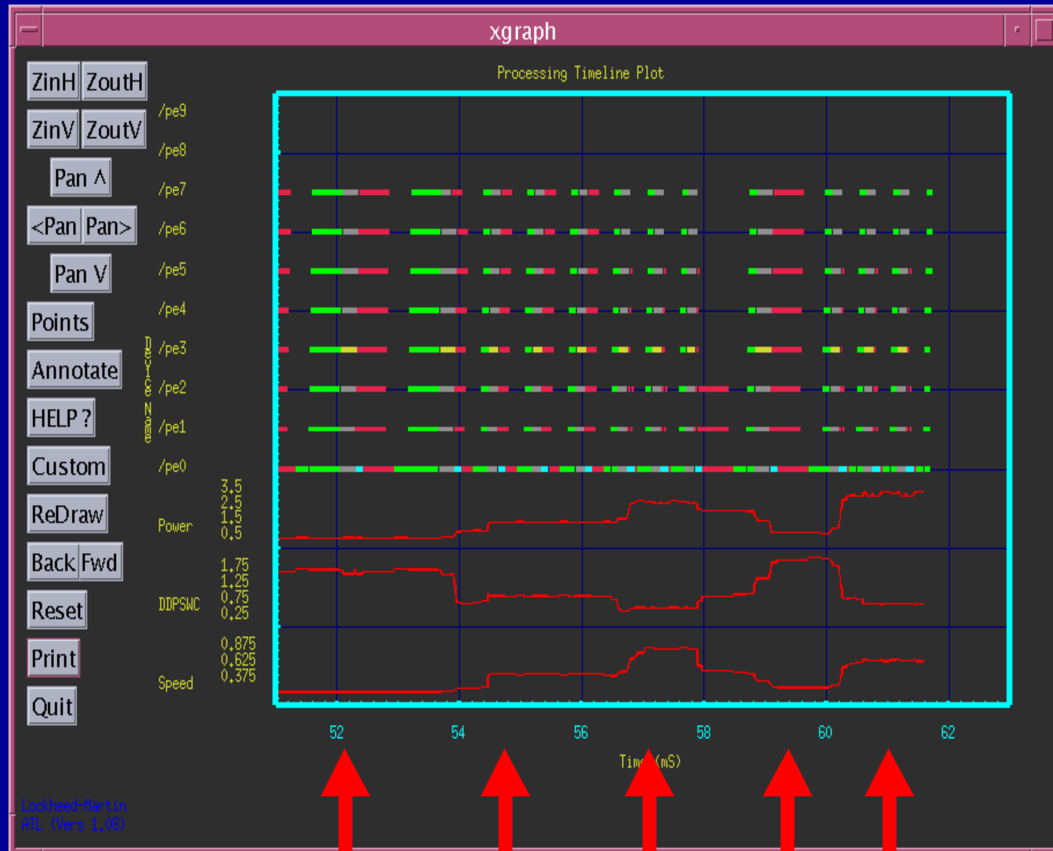
Processor Architecture and Environment

This graphic illustrates a representative processor architecture and an associated CSIM visualization environment. The core CSIM capability has been augmented with a dynamic scheduler that can apply complex selection criteria to the scheduling process. In this example, these complex selection criteria are encapsulated as several "modes"; the buttons on the lower right are used to interactively switch between the modes. In addition, any of the processors can be "killed" or returned to the simulation, facilitating the evaluation of failover and similar analyses. Illustrative results are shown in the following slides.



Dynamically Reconfigurable Architectures

- **Real time on-demand dynamic allocation of computational resources**
- **Each task/component (i.e. fft, fir) is abstracted by several parameters (i.e. throughput, latency, power, size, etc.)**
- **Each task may have several differently optimized implementations**
- **An online library of implementations is selected**
- **At run time the implementation best matched to the current selection criteria is executed**
- **For this example, the maximum throughput to minimum power dissipation ratio is improved >10X versus standard practice**

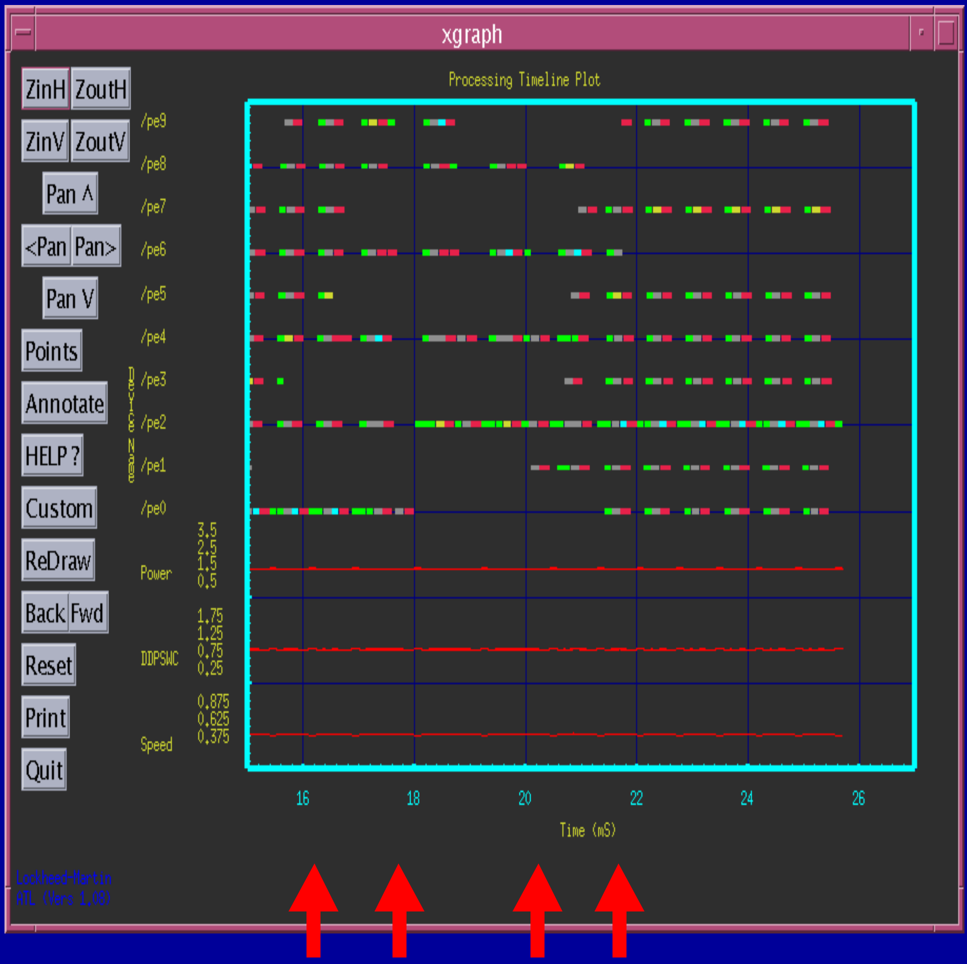


Power-driven scheduling; “LoPwr”	Assigned task scheduling, “Base”	Max speed-scheduling, “Fastest”	Complex criteria driven scheduling, “DDPSWC”	Assigned speed scheduling, “Fast”

SWEPT improvement >10X vs standard practice

Dynamically Reconfigurable Architectures

- **Validation and verification of next generation processor architectures**
- **Any processor may be temporarily or permanently removed from the architecture**
- **Processors may be returned to the architecture**
- **Facilitates development and analysis of failover/fault adaptation methodologies**
- **Extends multidimensional optimization to architectures with intermittently inactive components (especially useful for throughput/ power trades)**



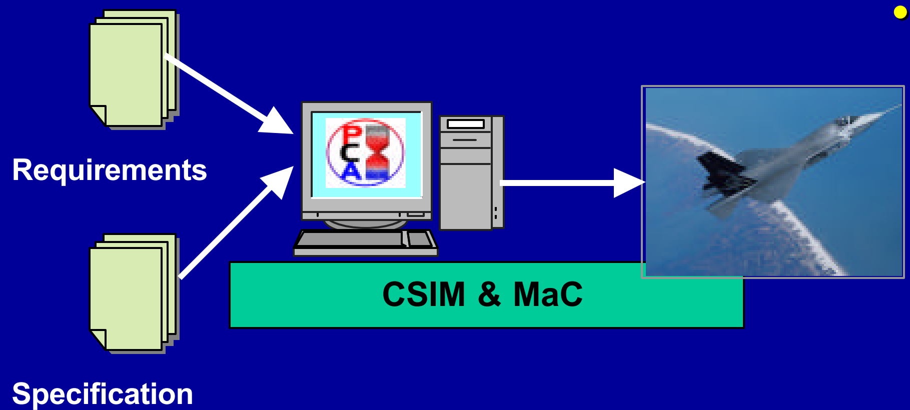
Processors faulted/ switched out

Processors returned to operation

Other Applications of CSIM

Program	Description	Customer	Key Technology
VNS	Network attack simulator for training IA operators	US Army CECOM	Token-based performance modeling, HLA
AMRFS	Agent-based resource management	ONR	Intelligent agents, dynamic scheduler
Advanced Surface Ship Model	Computing infrastructure model	LM NE&SS-Moorestown	Token-based performance modeling, pre-emptive multitasking CPU models
Avionics Mission Computing System	Model of JSF-Integrated Core Processor	LM NE&SS-Egan	Token-based performance modeling, hardware/ software co-simulation
Wireless Mobile Networks	Dynamic ad hoc routing behaviors	DARPA (XGComms) US Army CECOM (WIN-T)	Abstract propagation and arbitration models, dynamic routing algorithms

Run-time Environment and Design Application for Polymorphous Technology Verification & Validation (RE-ADAPT V&V)



- **New Ideas**
  - Methodology for run-time detection of requirement violations
  - Framework for automatic generation of monitoring and checking components
  - Dynamic run-time corrector to force reconfiguration into a safe state

- **Impact**
  - Design-Time Modeling and Simulation Environment for Verification and Validation (V&V) of PCA enabled applications
  - Run-Time Monitoring for PCA Enabled Application V&V
  - Approach Validation via application to PCA enabled avionics design

DARPATech Demo

Total active processor count display

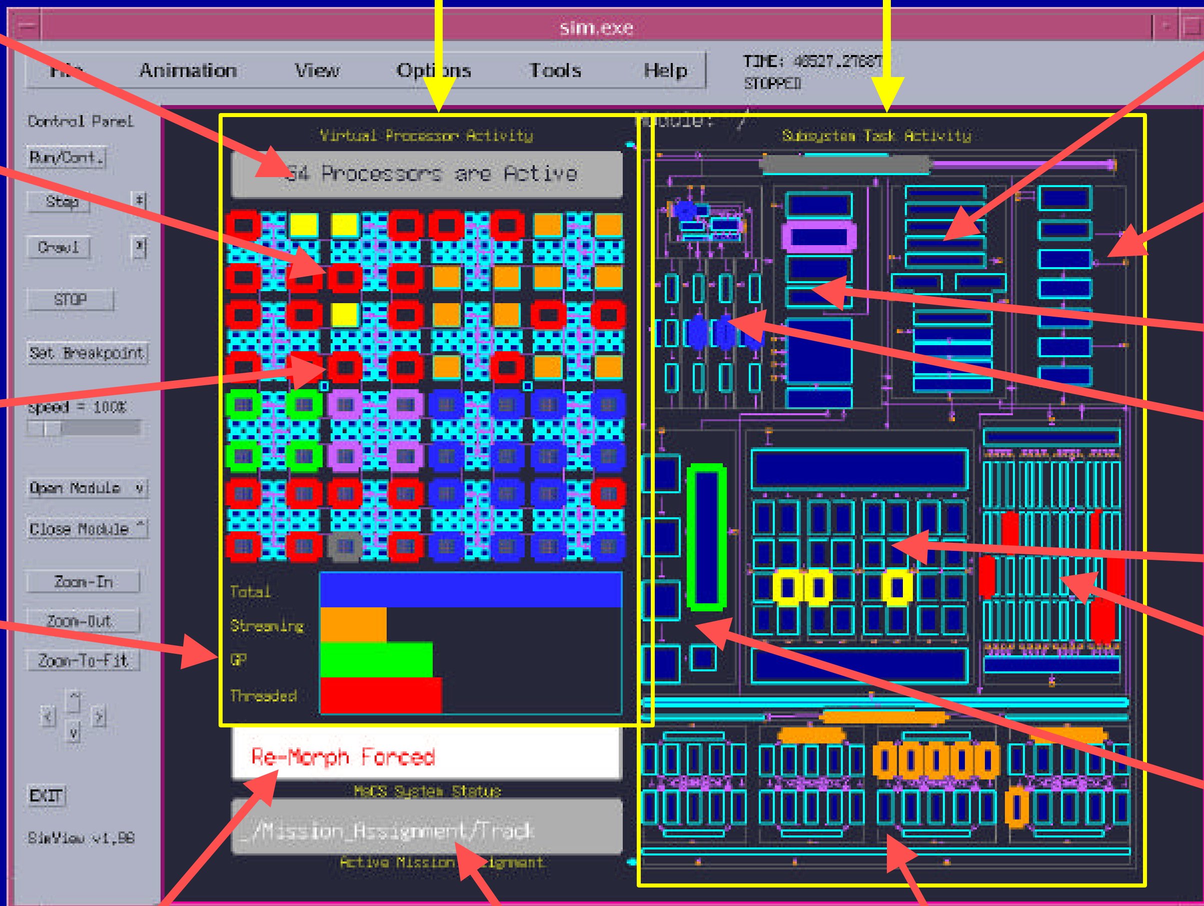
Stream Processors indicated by filled boxes

GP Processors indicated by outlined boxes

Dynamic bar chart indicating total active processors, active stream processor active GP processors and active threaded processors

PCA Virtual Processor State and Activity

System State and Task Flow



Mission Assignment

Threat Avoidance

Communi-cations

Flight Control

Imaging

Route Planning

Self Test and MaCS

MaCS messages and status

Mission status

RADAR Tasks

Real-time Systems Group, University of Pennsylvania