Session 1: Novel Hardware Architectures

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High Performance Embedded Computing

- A Historical Perspective -

1997	1998	1999	2000	2001	2002

Computing Systems

Intel Paragon

- 50 MHz i860
- 256 nodes
- 0.07 Mflop/s per watt

STAP Processor

- 40 MHz ADSP 21060
- ~1000 nodes
- 12 Mflop/s per watt

AFRL High Performance Computing System

- 333 MHz PowerPC 603e
- 384 nodes
- 39 Mflop/s per watt

Improved Space Processor Architecture

- 266 MHz PowerPC 603e
- 20 nodes / 40 PowerPCs
- 30 Mop/s per watt

Mk48 Torpedo CBASS BSAR

- 80 MHz ADSP 21160
- 12 nodes
- 91 Mflop/s per watt

- Heterogeneous processors
- 100s of Mflop/s per watt to Gflop/s per watt

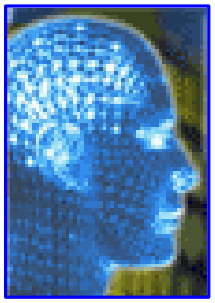
Enabling Technologies

- Vector Signal and Image Processing Library 1.0 API
- MPI-RT standard
- Adaptive Computing Systems & Reconfigurable Computing
- Data Reorganization forum
- VLSI Photonics
- High-Performance CORBA
- Polymorphous Computing Architectures
- Fault tolerant/fault recovery
- High-Performance Embedded Interconnects
  - InfiniBand
  - Serial RapidIO
- Parallel MATLAB
- Cognitive Processing
- Integrated ASICs, FPGAs, PIM, and/or prog. devices
- Real-Time Linux
- VXS: VMEbus Switched Serial

Session 1: Papers Highlights

Cognitive Information Processing Technology (Invited)

Zach Lemnios / DARPA / IPTO



Cognitive Systems Goals

- Reason
- Learn
- Explain
- Be Aware
- Respond

MIND: Scalable Embedded Computing Through Advanced Processor in Memory (PIM) Architecture(Invited)

Tom Sterling / CalTech / JPL

Processor in Memory

- 10x - 1000x memory BW
- 4x – 10x reduced latency
- >10x power efficiency
- PIM for unmanned space vehicles

MONARCH: A High Performance Embedded Processor Architecture with Two Native Computing Nodes

John Granacki / USC / ISI

Integrated Heterogeneous Processors

- System on a chip architecture
- Flexible VLSI device for stream front-end and threaded back-end processing

DARPA DIS Embedded Computing Benchmarks for Critical Defense Signal Processing Applications

Stephen Shank / Lockheed Martin

Data Intensive System Benchmarks

- Novel DIS architectures
- Applications: pulse comp., sidelobe canceller, digital target generation, and beam steering