

MIND: Scalable Embedded Computing through Advanced Processor in Memory (PIM) Architecture

Dr. Thomas Sterling
California Institute of Technology
CACR MC158-79, 1200 E. California Blvd.
Pasadena, CA 91125
(626) 395-3901
Fax (626) 584-5917
tron@cacr.caltech.edu
USA
and
NASA Jet Propulsion Laboratory

Recent advances in semiconductor fabrication processes that enable the merger of CMOS logic and DRAM storage devices on the same silicon die are providing new opportunities in digital system architecture for, but not limited to, high end embedded computing. Processor in Memory (PIM) devices match the row-wide on-chip memory interface at the sense amps or row buffer with logic that is a significant portion (perhaps 256 bits) of the total innate row size (e.g. 2048 bits) to deliver processing throughput comparable to the memory read access burst rate. PIM accords many advantages to computing structures compared to conventional system architectures. Through multiple partitions of the memory stacks as well as direct access to the entire row buffer of each stack, memory bandwidth may be increased by between one and three orders of magnitude. By direct placement of arithmetic units at the memory stack row buffer, access latency can be reduced by between a factor of four and ten. Power consumption will be dramatically reduced, perhaps by more than an order of magnitude, due to the use of much simpler processor design and because on-chip operations do not require use of external I/O pin drivers. Because of the multiple partitions and the wide ALUs per memory partitions, peak performance can be very high in spite of the moderate clock rates (approximately 500 MHz today) of PIM CMOS logic. These many advantages over conventional system architecture make PIM a contender for embedded computing but they alone are insufficient for the purpose.

MIND (Memory, Intelligence, and Networking Device) is a new generation of PIM architecture under development by the NASA sponsored Gilgamesh project to exploit PIM for unmanned space vehicles. The application of scalable PIM-based high performance embedded computer architecture to the challenge of autonomous spacecraft control and mission science is motivated by the opportunity to provide low cost platforms capable of decades-long missions possibly beyond direct operational management. A critical part of achieving dramatic improvement in spacecraft cost is the reduction of downlink bandwidth that may result. Much of the weight and cost of a deep space platform is related

to supporting high bandwidth in order to send down all the raw data acquired through onboard instrumentation. As remote sensor technology improves, the wealth of data assimilated by vehicle science packages escalates and the need for every greater downlink capability expands proportionately. But this assumes that all of the data measured by spacecraft sensors is shipped back to Earth.

The weight and cost of the spacecraft is tightly correlated with the downlink bandwidth and the distance to be transmitted. The size of the paraboloidal high-gain antenna, the power amplifier required to drive it, the power supply required to power it, the size/weight of the spacecraft framework to support all these, the size/weight of the attitude thrusters to maneuver the implied mass, the weight and size of the volatiles and their storage tanks for the thrusters, and the size of the booster rocket and its fuel to lift the entire payload in to space and on a trajectory to the outer reaches of the solar system all combine in multiplicative manner to determine mission cost. But if the science product can be computed in situ from the raw data, much less information need be sent back to Earth with a commensurate reduction in required downlink bandwidth and savings in spacecraft cost. This is a controversial position. Many scientists demand that they have access to all measurements. But the tradeoff ultimately is science per dollar. And if we can fly more missions on the same budget, then the end good may be best served by those same scientists placing intelligent algorithms in the vehicle to act as their surrogate in looking for the anomalies that so often lead to new insights. A simple example is an asteroid mapping mission where today we send back all pixels of everyone of a hundred thousand or more photographs taken of a single asteroid when all we actually want is the map; a potential reduction of downlink data of four orders of magnitude. PIM-based scalable HPEC system technology may enable in situ science product computation and the consequent reduction in mission cost.

Of equal importance is the PIM-based space computing which may enable new classes of missions that are impractical today through a combination of extreme reliability and highly intelligent autonomous control. Highly replicated fine grain structures such as arrays of PIM chips each comprising multiple memory/processor nodes can permit continued system operation even as individual nodes experience hard failures. Graceful degradation allows homogenous parallel architectures to reduce capability over time in response to faults without loss of functionality, at least up to a point. Missions up to a few decades may be made possible through PIM based high end embedded systems permitting long term exploration of the outer planets and their moons as well as the first pathfinding ventures in to interstellar space. High end computing in space will also facilitate very smart control algorithms and strategies that can support missions that would not be possible without fully autonomous mission planning and vehicle operation. The Pluto Express mission, if carried out will result in a fly-by of the Pluto system of less than two hours after more than a decade of transit time and a transmission latency of almost six hours. By the time scientists see their first experimental data, the spacecraft will have exited the

system. There will be no chance to provide direct control of the data gathering aspects of the mission. The spacecraft will have to make all of the decisions literally on the fly. Even more challenging are missions under consideration to explore the oceans underneath the ice crust on the Jovian moon, Europa. Throughout this potentially long and complicated mission, the extraterrestrial submarine will be out of contact with Earth and must respond to exigencies perhaps beyond our imagination, let alone a priori planning. High end embedded computers on board such submersible spacecraft will make such hidden missions possible.

MIND is an advanced PIM architecture under development by the Gilgamesh Project under the sponsorship of the NASA CICT Program (managed by Ames Research Center) and conducted at the Caltech Jet Propulsion Laboratory. MIND is intended to serve in two highly distinct roles. One is as a smart memory for ground based supercomputers to accelerate data intensive computations and increase overall system efficiency. The second is to provide a medium for achieving high performance, high availability computation in space for low cost autonomous long term space missions as described above. MIND incorporates innovative architectural features not found in a single PIM component. These include multithreaded execution control, message driven remote computation and communication, virtual memory and task name spaces with distributed address translation, active power management, real time threads, and mechanisms in support of fault tolerance strategies. MIND permits highly scalable systems through these mechanisms and methods while providing practical solutions to the challenges of size, weight, and power. This talk will discuss the challenges addressed by MIND and describe the architectural innovations embodied by the MIND design.