

HPEC-SI Demonstration:
Common Imagery Processor – APG-73 Image Formation

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This talk discusses the application of standards-based software techniques to the *operational* military signal and image processing software contained in the Common Imagery Processor (CIP). The CIP APG-73 software port is the first demonstration executed under the High Performance Embedded Computing Software Initiative and is a collaborative effort involving MITRE and Northrop Grumman, the CIP developer.

The CIP is the primary signal processing element of the Common Imagery Ground Surface/System (CIGSS) architecture. The CIGSS architecture defines interoperability and commonality requirements for ground based image processing and exploitation systems. The CIP role in the CIGSS architecture is to interface with collection, dissemination, and management elements via a local area network to provide exploitable images to forward stations.

The APG-73 is the SAR component of the Advanced Tactical Airborne Reconnaissance System (ATARS). The ATARS is installed on F/A-18D Hornets as an asset for the Marine Expeditionary Forces. The APG-73 sensor data is either recorded to an on-board digital tape for later processing or transmitted to a ground platform for immediate processing via a Common Data Link. In general, APG-73 SAR processing will be performed by a Marine Tactical Exploitation Group ground station, but any ground station containing a CIP is capable of processing the sensor data. Examples of other CIP deployed ground stations include the Army's Tactical Exploitation System and the Navy's Tactical Input Segment.

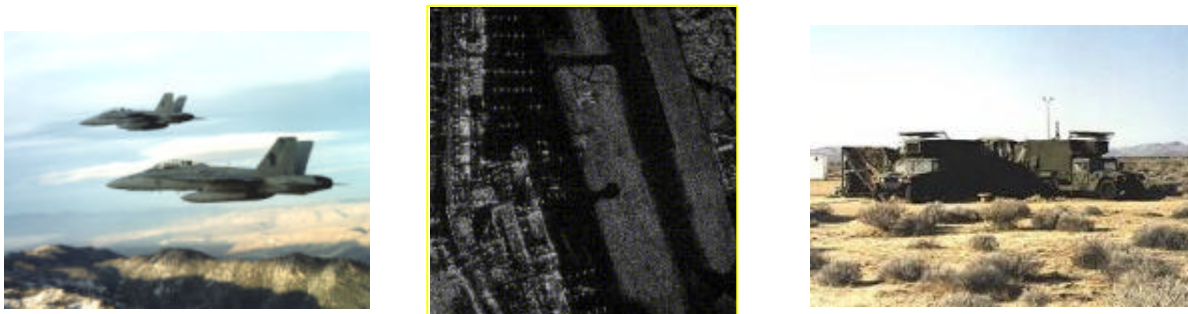


Figure 1. F/A-18D Hornets, Demonstration Output Image, Tactical Exploitation Group

The demonstration involves the development of a distributed-memory parallel implementation of the CIP APG-73 spotlight SAR image formation that uses the Vector Signal and Image Processing Library

(VSIPL) and the Message Passing Interface (MPI) application programming interfaces (APIs). These APIs are intended to enhance the portability of application software developed for real-time embedded applications. The CIP APG-73 Image Formation is currently implemented using shared-memory techniques on high-performance server class machines from vendors such as SGI and COMPAQ.

By using portable standards, the software examined could potentially realize the “write once, run anywhere” vision. For an embedded system, this means that a program could be written and functionally tested on a workstation or commercial server and then ported to the desired embedded platform. Truly portable software will eliminate the cost of migrating systems to new hardware architectures, thus allowing immediate gains to be realized through model year improvements. The software developed in this experiment will bridge the gap between HPC and HPEC portability by employing the Message Passing Interface (MPI). Furthermore, using compiler directives, one baseline will support the shared-memory, distributed-memory, and the vectorized software. This allows many different version of the CIP software to be compared providing realistic comparisons between different technology options.

The first task in this effort was vectorizing the original APG-73 software. Initial profiling of the APG-73 kernel performance identified the most important candidates for VSIPL application. Identified kernels include range and azimuth compression, inverse weighting, and side-lobe clutter removal. The original software is written in ANSI C and uses pointer arithmetic and loops to perform common vector operations. The techniques used to replace the original software with VSIPL routines along with the difficulties encountered with shared-memory software will be discussed. The impact of VSIPL application will be evaluated by comparing the software lines of code and the run-time performance of the resulting standard-based software against the existing operational server based software.

While standard software APIs are the ideal solution to realize portable software their lack of maturity or acceptance sometime requires alternative/interim solutions. For example, standard VSIPL is hand optimized on a limited number of platforms, mostly HPECs. VSIPL can be used on any platform that supports the ANSI C run-time environment by using a freely available reference implementation, but the performance will not be optimal for that particular platform without additional optimizations. Alternative solutions will be discussed where they have been applied in the CIP demonstration.

The second task in this effort is the replacement, in software, of shared-memory techniques for achieving parallelism with equivalent distributed-memory techniques. The APG-73 software employs the shared-memory technique of compiler pragma's to direct the parallelism of loops in the main program. These compiler directives will be replaced with Data Reorganization Interface (DRI) routines along with the associated loop structure modifications. The DRI is a higher level abstraction for distributed data objects and is intended to reduce the software development complexity associated with message passing on distributed-memory multicomputers. To ensure portability a baseline DRI layered on top of MPI will be used where optimized alternatives are not available. Again, the impact of DRI application will be evaluated by comparing the resulting standard-based software against the existing operational server based software.

