DARPA Data Intensive Systems (DIS) Embedded Computing Benchmarks for Critical Defense Signal Processing Applications - Presentation

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Abstract

This briefing describes an effort to implement advanced embedded signal processing algorithms, including radar Pulse Compression, Coherent Sidelobe Cancellation (CSLC), Digital Target Generation (DTG), and embedded Phased Array Beam Steering Control (BSC), using Data Intensive Systems (DIS) computing architectures developed by DARPA. Of particular interest is a comparison of these key DoD processing algorithms executed on a conventional embedded processing architecture, such as embedded PowerPC G3 or G4 clusters, with execution on embedded DIS processor architectures. The goals of this effort were to:

- Demonstrate critical embedded DoD signal processing benchmarks using DARPA Data Intensive Systems (DIS) technology-based architectures
- Compare performance, size, and cost with existing embedded COTS processor architectures
- Demonstrate the ability to program the embedded DIS-based architectures through the use of industry standard APIs and Portability Standards, such as VSIPL, MPI, and DRI
- Demonstrate the key embedded DIS technology, running a subset of the Benchmarks, for key US and foreign Defense Department representatives
- Develop a plan to transition DIS-based processors into embedded DoD tactical systems

This new technology, being promoted by the DARPA Data Intensive Systems Program, promises to provide alternative embedded computing architectures to classical PowerPC or Pentium-based architectures. The DIS architectures can provide for a processing core that is closely coupled to and on the same die as the memory structure, thus providing for more powerful data access in a data intensive systems application. The DIS embedded processor designs promise to save significant equipment space and to provide a lower cost solution by providing hundreds or even thousands of low-cost, high performance embedded processing engines, with memory, on a 6U size electronic module. By providing standard APIs and embracing emerging portability standards, we hope to eventually port legacy applications to new embedded DIS architectures.

In this briefing, we describe four embedded processing applications, Radar Pulse Compression, Coherent Sidelobe Cancellation (CSLC) for a phased array radar, Digital Target Generation for a real-time radar simulator/stimulator, and a phased array radar Beam Steering Control (BSC) architecture. Benchmark results will be provided that compare each representative benchmark algorithm, on both conventional embedded architectures (such as PowerPC) and DIS-type architectures. Finally, the results of a benchmark algorithm subset run on an actual DIS hardware architecture in summer 2002 will be presented.