The Raw Microprocessor: Enabling Embedded Signal Processing on a General Purpose Computer Architecture

Hank Hoffmann, Volker Strumpen, Anant Agarwal
MIT Laboratory for Computer Science

1.0 Introduction

The Raw microprocessor, under development at MIT's Laboratory for Computer Science, is designed to address the problem of leveraging the growing number of on-chip resources as wire delay becomes substantial [1]. Toward this end, Raw implements a scalable ISA which exposes the physical resources of the chip to software. By exposing the chip-level gates, wires, and pins, Raw gains the energy and performance advantages of application-specific integrated circuits (ASICs), while maintaining the programmability of a general purpose processor, thus making it well suited for the demands of embedded signal processing.

2.0 The Raw Architecture

The Raw chip is divided into a fabric of identical tiles, where each tile contains an in-order, single issue MIPS-derived processor, a 4-stage pipelined FPU, a 32 KB data cache, and programmable interconnects. The current prototype chip being developed is a four by four configuration of tiles, but the Raw architecture is designed to seamlessly scale up to a thirty-two by thirty-two configuration.

The interconnects on each tile are exposed to the user through the Raw ISA, thus allowing the application developers to directly access to the wiring resources of the processor and to orchestrate the transfer of data between functional units on the tiles. The replicated functional units mean that a single Raw chip is capable of executing sixteen operations (load, store, ALU, FPU, etc.) every cycle, while the exposed network connections make it possible to keep these replicated functional units fully utilized. For our prototype ASIC implementation, clocked at 250 MHz, this gives us a peak floating point rate of 4 GFLOPS. This compares favorably with Analog Devices' TigerSHARC ADSP-TS101S, which has a peak performance of 1.5 GFLOPS [2].

3.0 Developing Signal Processing Applications on Raw

The Raw architecture allows signal processing development at a number of levels. First, for truly demanding computational requirements, a large fabric of Raw tiles can be used

and the programmer can develop applications directly on top of the Raw ISA. Such an approach allows almost full floating point utilization for computations with regular communication requirements. Indeed, we have found that for beamforming, fir filtering, and discrete fourier transforms, such an approach yields 91-100% asymptotic floating point efficiency. In addition, the exposed nature of Raw's interconnects allows programmers to hide completely hide the latency of difficult communication patterns, such as the corner turn (see last entry of Table 1 on page 2).

Furthermore, it is also possible to develop a signal processing library that exploits Raw's exposed architecture while simultaneously hiding those low-level details from a programmer. Such an abstraction trades a small amount of efficiency for a large increase in programmer productivity, as the programmer is then freed from worrying about the low level details of programming Raw's interconnects. Currently, a higher level library is being developed to provide an abstraction layer that still enables Raw to meet high throughput requirements, and we anticipate having those results by the end of July.

Many key signal processing kernels have already been hand coded for the prototype version of Raw mentioned above, and the achieved performance on our cycle accurate simulator is listed in Table 1, thus demonstrating that Raw is a suitable architecture for embedded signal processing. In addition, this work suggests that software-exposed, tiled architectures in general may be extremely useful for signal processing.

TABLE 1. Asymptotic Performance of Selected DSP Kernels on the Raw Prototype

	Performance	
Kernel	**% of Peak**	**GFLOPS**
16 tap FIR Filter	**98**	**3.94**
4 x 4 * 4 x N Matrix Multiply	**94**	**3.76**
16 point DFT	**100**	**4**
2 tap FIR Filter to 4 channel, 2 beam beamformer with corner turn	**91**	**3.3**

4.0 References

[1] Waingold et al., "Baring it All to Software: Raw Machines," Computer, vol. 30, no. 9, Sept. 1997, pp. 86-93

[2] "Analog Devices Delivers Industry's Highest Performance Floating-point DSP Operating at 250 MHz," press release, Feb. 2002, www.analog.com/pressrelease/prdisplay/0,1115,448,00.html