High Bandwidth Reconfigurable Embedded Daughter Card Accelerator

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Abstract

The use of FPGAs to operate as hardware accelerator nodes in high performance embedded processing systems or as front-end sensor preprocessors is in use in a number of formats. Previous experience with this approach has shown that, in order to achieve high performance and efficiency in many of the data streaming applications of sensor processing algorithms, the network data bandwidth at the FPGA processing node (consisting of FPGA(s), local memory, and network I/O) needs to be matched with the FPGA local memory bandwidth.

This paper describes the implementation of a daughter card format FPGA based accelerator node, capable of providing the matched bandwidth described above, in terms of the design and application results.

Referring to Figure 1, the daughtercard design consists of multiple Race++ network ports, an FPGA based processing element, and over 5 GBytes/sec of local memory bandwidth.   The daughtercard provides the acceleration of the very high throughput operations typical of military sensor data processing.   An Automatic Target Recognition ATR) algorithm is implemented as the application.

Figure 1
ATR Algorithm Implementation Block Diagram
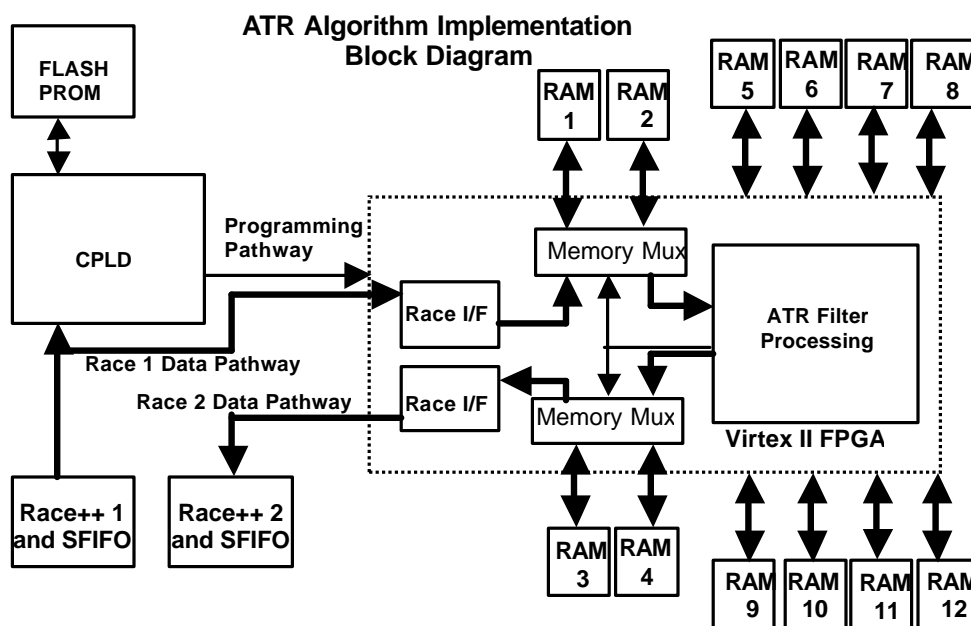
The daughter card design is formatted to be compatible with Race++ motherboards, and is used as an alternate processing node to the Power PC/Altivec node. The processing engine is a six million gate Xilinx Virtex II FPGA, surrounded by twelve 32-bit wide banks of 133 MHz SSRAM memories. The daughter card has two Race++ ports connected to the FPGA, allowing the node to be reconfigured in a number of data I/O schemes, depending on the application: a dataflow (data streaming in one port and out the other), or coprocessor (two parallel ports) architecture. Additional key features include the ability to store multiple FPGA configuration images on the daughter card; the ability to download new FPGA configuration programs over the Race++ interface, providing in-system reconfiguration and adaptability; and software reprogramming of the processing clock frequency to provide performance vs. power management.

This paper describes the implementation and application of the accelerator to an end-to-end Automatic Target Recognition (ATR) algorithm running on a heterogeneous configuration of PowerPCs and accelerators. Programming techniques used to integrate the accelerator into a heterogeneous processing system will be discussed. Portable software techniques for integration of the accelerator function calls (performing high throughput filtering) within an existing body of C-code are described. Programming techniques and lessons learned using the latest Xilinx tools are also presented. Metrics comparing performance of this high bandwidth daughter card approach to programmable approaches are discussed, and the need for and benefits of the high bandwidth features are highlighted.