A Comparison of Two Computational Technologies for Digital Pulse - Compression

Abstract Submitted by
Michael J. Bonato
Catalina Research Inc.

Short development cycles, program cost constraints, and an ever increasing desire for improved system performance considerations are forcing engineers to look for efficient ways to build radar receivers. This paper will focus on the abilities of today's "platform FPGA" technology and will compare it to approaches utilizing dedicated vector processing ASICs so that an engineer can understand the benefits of each technology and make informed decisions when designing a radar receiver.

The common radar operation of digital pulse compression, which is a matched filtering function, will be used to compare the two processing technologies. The paper will first focus on algorithmic approaches to the pulse compression problem, and provide an in-depth look at time domain techniques (Finite Impulse Response Filters). This discussion will be followed by a similar investigation into frequency domain processing (e.g. Fast Fourier Transform) based methods of matched filtering.

Of particular interest will be a review of FIRs and sectioned convolution techniques, leveraging MATLAB for illustrative purposes. As part of this review, the number of operations required for each computational approach will be counted in an effort to accurately gauge the efficiency of each candidate method for pulse compression.

These results will help define an optimal, common, algorithmic approach to pulse compression such that a typical real-world radar problem can be used to help fairly gauge the computational capabilities of platform FPGAs and dedicated vector processors.

Given a defined efficient computational approach to the implementation of pulse compression, the paper will then present how the function maps into each processing technology. The goal is to understand both the benefits and drawbacks of each hardware approach with respect to critical system trade-offs such as dynamic range, precision, the time-bandwidth product of the radar transmit waveform, and overall performance.

For a defined time-bandwidth product, the paper will size a pulse compression algorithm for both processing technologies, taking into account the critical consideration of dynamic range and precision. It will be shown how the number of bits required for the computations greatly dictates the attractiveness of a chosen processor technology approach.

At that point, the paper will quantify the achievable system performance by calculating the Pulse Repetition Frequency (PRF), a common radar metric, supportable by each processor solution

given a typical time-bandwidth product for the transmit waveform and the capacity of the processor in question.

Key to this processor comparison is the breadth of supporting logic and components necessary to allow the platform FPGA, or the vector processor, to handle the computations in a real-world application. In order to take this critical consideration into account, this paper will also review a handful of COTS board architectures featuring either FPGA-based or vector-processor computational nodes. The number of supporting components on each board will be noted and figured into the overall analysis.

Related closely to the board investigation is the application code development methodology for realizing a pulse compression algorithm on the hardware platform in question. After all, the best processing approach in the world is useless if one cannot realistically develop an application for it. The tool flows options for both an FPGA-based solution and a vector processing solution will be reviewed and compared.

The conclusion of this paper will summarize the overall findings, and tabulate them in such a way that an engineer can easily refer to the information to make intelligent, informed decisions about how to leverage the right tool (FPGAs or dedicated vector processors) for the job of radar pulse compression, given a set of target system parameters.