Partitioning Computational Tasks within an FPGA + RISC - Heterogeneous Multicomputer

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Field Programmable Gate Arrays (FPGAs) used as reconfigurable computing elements have achieved an order-of-magnitude performance improvement over the best RISC processors for selected computational tasks. Many other computational tasks are better suited to RISC processors such as the PowerPC® with AltiVec. By building a heterogeneous multicomputer with both FPGA computing elements and RISC computing nodes, better system performance within embedded-system constraints of size weight, and power, may be achieved than is possible with a homogeneous system using only one of these computing technologies.

The key to achieving these benefits is to successfully map the computational tasks onto the heterogeneous computing elements within the multicomputer. But how do you do this? Many factors affect the choice of where to deploy a computational task:

- Raw performance improvements that FPGAs are capable of varies widely by algorithm or computational task. Often FPGA benefits are best for computational requirements that "break" the RISC processor architecture.
- FPGA power dissipation varies widely depending on the algorithm and utilization.
- Raw-parts cost of computationally interesting FPGAs is greater than that for the PowerPC; this must be offset by other benefits.
- Application development for FPGAs takes longer than for PowerPCs.
- Computational capability may be left on the table when the I/O to that processing element is the limiting factor.

This presentation will examine the trade-offs using an example application that includes an algorithm well suited for FGPA-based computing. Portions of the application were well matched to PowerPC compute nodes, while other portions were better suited to FPGAs. An FPGA demonstration board was built to add FPGA computing to the switch-fabric multicomputer, and the application was developed for the heterogeneous FPGA and PowerPC system. Detailed results will be presented showing a 50x improvement for the key backprojection algorithm. For the overall application, this resulted in a 4X performance improvement with a simultaneous 4-6X improvement in size over a PowerPC-only solution for the overall signal processing subsystem.

This presentation examines how the decisions were made to partition the reconstruction problem between the PowerPC nodes and the FPGA nodes. The types and characteristics of each of the computational steps and why they were best suited for a particular node type will be discussed. Finally, some thoughts will be presented on how these findings can be generalized to other embedded-computing problems.

Format: oral presentation

Topic Areas:

- Future Program Office Needs
- Reconfigurable Computing for Embedded Systems
- Advanced Digital Front-End Processors