

# A High Speed Signal Processing System -

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## Extended abstract

### 1. System Concept

In modern array radar signal processing applications the processing demands range from tens of GFLOPS to several TFLOPS. The array signal processing calculations are to the largest extent FIR filters, FFTs, QR-decompositions, SV-decompositions, matrix by matrix multiplications, and other similar calculations. These properties make the applications naturally lend themselves to systolic array implementations. However, using systolic arrays means that generality is traded for increased performance. In most cases the processor system will be specialized towards one specific data size and type of algorithm, which is a problem for a multipurpose radar where both matrix sizes and algorithms change during operation. At the other end of the architectural scale, there exist commercial distributed memory MIMD (Multiple Instruction streams, Multiple Data streams) systems, such as the Mercury RACE, which are highly flexible but they can not provide enough computational density.

In a research project, carried out in cooperation with Halmstad University, Sweden, we have designed a system which is in between the pure systolic array and the distributed memory MIMD system. It is a system which is specialized toward array signal processing and matrix calculations. It can cope with changes in matrix sizes and algorithms, and at the same time it is scalable in performance. To achieve this, as much generality as possible is kept, while not sacrificing performance. The system is a combined MIMD and SIMD (Single Instruction stream, Multiple Data streams). The MIMD system level provides the high level flexibility, while the SIMD module level provides performance density. The system's integral components are described below.

### 2. The System

The High Speed Signal Processing (HSSP) system, see Figure 1, consists of 4 - 40 interconnected processing nodes on up to five cassettes. The system performance scales to 1 TFLOPS with less than 1 kW estimated power consumption. The processing nodes are based on SIMD processor arrays, which provides for high performance in matrix calculations. The system is further described below.

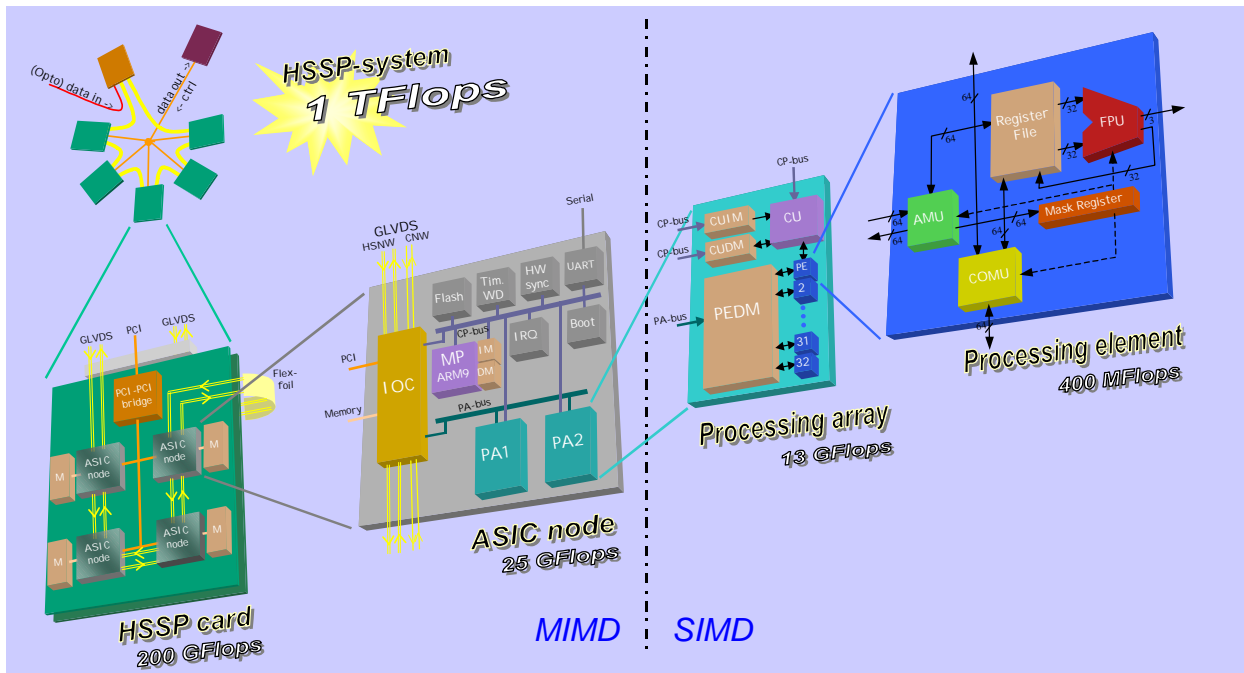


Figure 1: HSSP system overview.

## 2.1 HSSP system

Five HSSP cards (cassettes) comprising a high speed ring network, a utility bus, a front-end (FE) with opto-interface, and a back-end (BE) with utility bus interface

Performance scales to 1 TFLOPS

## 2.2 HSSP cards (cassettes)

8 ASIC nodes per cassette, 4 on each side. The nodes are interconnected by a double direction GLVDS ring network with separate channels for data (1.6 GB/s) and control (100 MB/s). The nodes also interconnected by a PCI utility bus. DRAM. Performance: 200 GFLOPS

## 2.3 ASIC node

The ASIC node (0.13  $\mu\text{m}$  process) is based on two processor arrays, acting as co-processors for matrix computations, which deliver the performance. The Master processor, which is a IP-core running a commercial RTOS, controls the node. The node also holds an I/O-processor (DMA, data transformations, etc.) and support functions (boot, UART, timer, etc.). Performance: 25 GFLOPS

## 2.4 Processor array (PA)

A processor array has 32 processor elements with 32 kB memory each, interconnected in a ring topology. The processing elements are controlled by a common control unit (SIMD). 400 MHz clock. Performance: 12.5 GFLOPS

## 2.5 Processing element

A processing element has 64 register file with 32-bit registers, 4 read and 3 write ports

The processing element is based on a 4 stage pipelined FPU, IEEE 754 single precision. It can communicate with its north and south neighbors. 64 bit memory access with possibility to load and store in a skewed manner, 3.2 GB/s bandwidth. Performance: 400 MFLOPS

## 3. Development Environment

The software development environment, see Figure 2, is to largest possible extent based on commercial components.

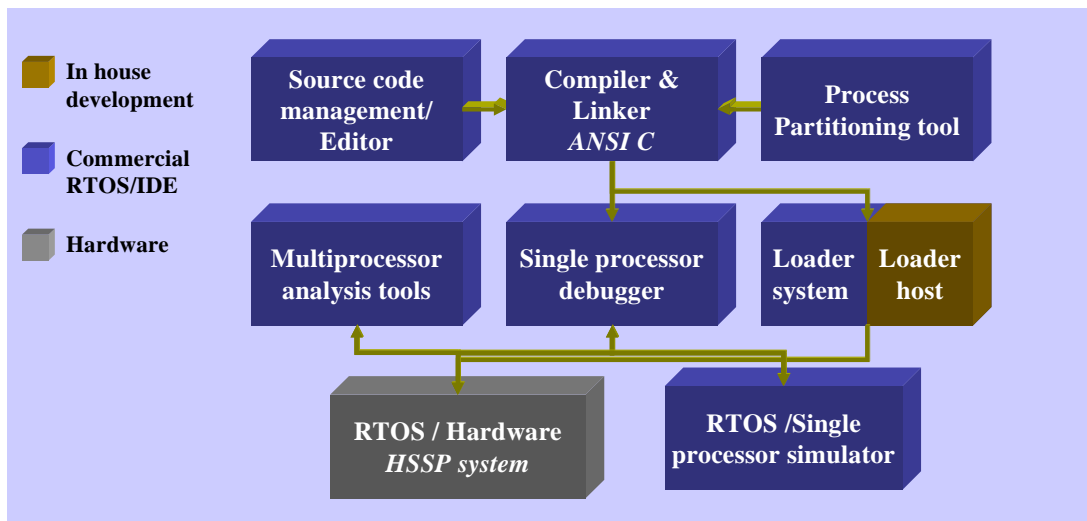


Figure 2: Commercial integrated developed environment.

## 4. Summary

We have designed a signal processing system that meets the requirements, including tight size and power constraints, from future multichannel fighter radar systems.