High Performance Embedded Computing Workshop

20 – 22 September 2005

AGENDA

20 – 22 September

Workshop at a Glance

Day 1 20 September	Check-in/Setup:	0730
		Keynote Address
	Sessions:	**Session 1**: Advanced Hardware **Poster / Demo A**: FPGAs Everywhere **Session 2**: Hardware Architecture and System Metrics **Focus 1**: Algorithms and FPGAs *(Session 2 and Focus 1 run in parallel)*
	Adjourn:	1720
		Reception (Burlington Marriott) **Banquet Speaker** **Banquet**
Day 2 21 September	Check-in/Setup:	0730
	Sessions:	**Session 3**: Advanced Parallel Environments **Poster / Demo B**: High Performance Software Technologies **Session 4**: Award Finalists Session – Advanced Software
		Panel: Will Software Save Moore's Law?
	Adjourn:	1730
Day 3 22 September	Check-in/Setup:	0730
	Sessions:	**Session 5**: Standards Usage and Updates **Poster / Demo C**: Software Standards
		Session 6: Advanced Systems **Focus 2**: Hardware Tools and Network Technologies *(Session 6 and Focus 2 run in parallel)*
	Adjourn:	1650

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20 September

Day 1 at a Glance

0730	Check-in / Poster Setup / Continental Breakfast	
0830	Welcome	
0835	Keynote Speaker: Brig Gen Gary Connor / Hanscom AFB	
0905	Opening Remarks	
0915	Session 1: Advanced Hardware	
0925	Invited Speaker: Robert Graybill / DARPA IPTO	
0955	Invited Speaker: James Kahle / IBM	
1025	Break	
1140	Poster / Demo A: FPGAs Everywhere	
1235	Lunch (View Posters)	
	Auditorium	**Room S2-180**
1345	Session 2: Hardware Architecture and System Metrics	Focus 1: Algorithms and FPGAs
1355		Invited Speaker: Charles Leiserson / MIT
1525	Break (View Posters, 15 min.)	Break (View Posters, 15 min.)
1650	Invited Speaker: Douglass Post / HPCMO	
1720	Adjourn	
1800	Reception (Burlington Marriott)	
1845	Banquet Speaker: Michael Cusumano / MIT Sloan	
1930	Banquet	

0730 **Check-in / Poster Setup / Continental Breakfast**

0830 **Welcome**
David Martinez / MIT Lincoln Laboratory

0835 **Keynote Address**
Brig Gen Gary Connor / Hanscom AFB

0905 **Opening Remarks**
Robert Bond / MIT Lincoln Laboratory

0915 **Session 1: Advanced Hardware**
Robert Bond / MIT Lincoln Laboratory

0925 **Future of Embedded Software from an Historical Perspective** (Invited)
Robert Graybill / DARPA IPTO

0955 **Cell Processor** (Invited)
James Kahle / IBM

1025 **Break (View Posters)**

1040 **Applications Kernels on Graphics Processing Units: An Analysis of Hidden Markov Models, Support Vector Machines, Hyperspectral Imaging, and Latent Semantic Indexing**
Sean Ahern / Lawrence Livermore National Laboratory
David Bremer / Lawrence Livermore National Laboratory
* John Johnson / Lawrence Livermore National Laboratory
Holger Jones / Lawrence Livermore National Laboratory
Yang Liu / Lawrence Livermore National Laboratory
Jeremy Meredith / Lawrence Livermore National Laboratory
Sheila Vaidya / Lawrence Livermore National Laboratory
Candace Culhane / Department of Defense

1110 **Embedding Applications within a Storage Appliance**
Roger Chamberlain / Washington University

20 September *(Continued)*

1140 **Poster / Demo A: FPGAs Everywhere**
Michael Vai / MIT Lincoln Laboratory

1150 **Poster / Demo A Précis**

Poster A.1 **Super-FPGA: Overcoming Von Neumann to Save Moore**
Venkatesh Akella / University of California
Soheil Ghiasi / University of California

Poster A.2 **Mapping of a 2D SAR Backprojection Algorithm to an SRC Reconfigurable Computing MAP Processor**
Peter Buxa / AFRL, Sensors Directorate
LeRoy Gorham / AFRL, Sensors Directorate
Mathew Lukacs / AFRL, Sensors Directorate
David Caliga / SRC Computers, Inc.

Poster A.3 **Enhancing FPGA Based Encryption on the Cray XD-1**
Joseph Fernando / Ohio Supercomputer Center–Springfield
Dennis Dalessandro / Ohio Supercomputer Center–Springfield
Ananth Devulapalli / Ohio Supercomputer Center–Springfield
Ashok Krishnamurthy / Ohio Supercomputer Center–Columbus

Poster A.4 **A Superpipelined CORDIC Unit**
Michael Fitzharris / Drexel University
* Jeremy Johnson / Drexel University
Prawat Nagvajara / Drexel University
Servesh Tiwari / Drexel University

Poster A.5 **Real-Time FPGA Implementation of Adaptive Beamforming Using QR Decomposition**
Michael Gay / QinetiQ Ltd.

Poster A.6 **A Data-Driven SoC System for Embedded Continuous Speech Recognition**
Raymond Hoare / University of Pittsburgh
Kshitij Gupta / University of Pittsburgh
Jeffrey Schuster / University of Pittsburgh

Poster A.7 **Iterative Demodulation and Turbo Decoding for Distributed Radio Receivers**
Preston Jackson / MIT Lincoln Laboratory
Joel Goodman / MIT Lincoln Laboratory
Hector Chan / MIT Lincoln Laboratory

Poster A.8 **Automatic Mapping of MATLAB Code to Parallel FPGAs on the SGI Altix**
Michael Murphy / Silicon Graphics, Inc.
* Michael Raymond / Silicon Graphics, Inc.
Steve Reinhardt / Silicon Graphics, Inc.

Poster A.9 **Interface Techniques for Microprocessors Embedded Within FPGAs**
Joshua Noseworthy / Northeastern University
Miriam Leeser / Northeastern University

Poster A.10 **Parallel FFT and Parallel Cyclic Convolution Algorithms with Regular Structures and No Processor Intercommunication**
Marvi Teixeira / Polytechnic University of Puerto Rico
Miguel de Jesus / Polytechnic University of Puerto Rico
Yamil Rodriguez / Polytechnic University of Puerto Rico

20 September *(Continued)*

Poster A.11 **A Methodology for Exploring Finite-Precision Effects When Solving Linear Systems of Equations with Least-Squares Techniques in Fixed-Point Hardware**
Ramon Uribe / AccelChip Inc.
* Thomas Cesear / AccelChip Inc.

Poster A.12 **Rapid Prototyping of a Real-Time Range Compression Processor**
Michael Vai / MIT Lincoln Laboratory
Thomas Anderson / MIT Lincoln Laboratory
Albert Horst / MIT Lincoln Laboratory
Robert Gallagher / MIT Lincoln Laboratory
Larry Retherford / MIT Lincoln Laboratory
Tom Emberley / MIT Lincoln Laboratory
Preston Jackson / MIT Lincoln Laboratory
Cy Chan / MIT Lincoln Laboratory
Charles Rader / MIT Lincoln Laboratory
Huy Nguyen / MIT Lincoln Laboratory
Paul Monticciolo / MIT Lincoln Laboratory

1235 **Lunch (View Posters)**

20 September *(Continued)*

1345 **Session 2: Hardware Architecture and System Metrics**
Paul Monticciolo / MIT Lincoln Laboratory
Auditorium

1355 **A Next Generation Ultra-High Performance Scalable Processing Architecture for Embedded Defense Signal and Image Processing Applications**
Stewart Reddaway / WorldScape Defense, LLC
Rick Pancoast / Lockheed Martin MS2
Dhon Paulo / Lockheed Martin MS2
* Pete Rogina / WorldScape Defense, LLC

1425 **A VLIW Processor with Hardware Functions: Increasing Performance While Reducing Power**
Raymond Hoare / University of Pittsburgh
Alex Jones / University of Pittsburgh
Dara Kusic / University of Pittsburgh
Joshua Fazekas / University of Pittsburgh
Gayatri Mehta / University of Pittsburgh
John Foster / University of Pittsburgh

1455 **Implementations of Signal Processing Kernels Using Stream Virtual Machine for Raw Processor**
Jinwoo Suh / University of Southern California, ISI
Stephen Crago / University of Southern California, ISI
Dong-In Kang / University of Southern California, ISI
Janice McMahon / University of Southern California, ISI

1525 **Break (View Posters)**

1550 **The HPEC Challenge Benchmark Suite**
Ryan Haney / MIT Lincoln Laboratory
Theresa Meuse / MIT Lincoln Laboratory
Jeremy Kepner / MIT Lincoln Laboratory
James Lebak / MIT Lincoln Laboratory

1620 **A Relative Development Time Productivity Metric for HPC Systems**
Andrew Funk / MIT Lincoln Laboratory
Jeremy Kepner / MIT Lincoln Laboratory
Victor Basili / University of Maryland
Lorin Hochstein / University of Maryland

1650 **Mitigating the Risks of High Performance Computational Science and Engineering** (Invited)
Douglass Post / HPCMO

1345 **Focus 1: Algorithms and FPGAs**
Henk Spaanenburg / Advanced Principles Group, Inc.
Room S2-180

1355 **Unbounded Transactional Memory** (Invited)
Charles Leiserson / MIT

1425 **High-Performance FPGA-Based QR Decomposition**
Huy Nguyen / MIT Lincoln Laboratory
James Haupt / MIT Lincoln Laboratory
Michael Eskowitz / MIT Lincoln Laboratory
Birol Bekirov / MIT Lincoln Laboratory
Jonathan Scalera / MIT Lincoln Laboratory
Thomas Anderson / MIT Lincoln Laboratory
Michael Vai / MIT Lincoln Laboratory
Kenneth Teitelbaum / MIT Lincoln Laboratory

1455 **Pipelined Data Path for an IEEE-754 64-Bit Floating-Point Jacobi Solver**
Gerald Morris / University of Southern California
Viktor Prasanna / University of Southern California

1525 **Break (View Posters)**

1550 **Sparse Matrix-Vector Multiplication Kernel on a Reconfigurable Computer**
Sreesa Akella / University of South Carolina
Melissa Smith / Oak Ridge National Laboratory
Richard Mills / Oak Ridge National Laboratory
Sadaf Alam / Oak Ridge National Laboratory
Richard Barrett / Oak Ridge National Laboratory
Jeffrey Vetter / Oak Ridge National Laboratory

1620 **GPGP: General Purpose Computations Using Graphics Processors**
Naga Govindaraju / University of North Carolina at Chapel Hill
Ming Lin / University of North Carolina at Chapel Hill
* Dinesh Manocha / University of North Carolina at Chapel Hill

1720 **Adjourn**

1800 **Reception (Burlington Marriott)**

1845 **Banquet Presentation – The Software Industry: How Business Models Are Changing from Products to Services**
Michael Cusumano / MIT Sloan

1930 **Banquet**

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AGENDA

21 September

Day 2 at a Glance

0730	Check-in / Poster Setup / Continental Breakfast
0830	Announcements
0835	Session 3: Advanced Parallel Environments
0845	Invited Speaker: Vivek Sarkar / IBM Research
0915	Invited Speaker: Roy Lurie / MathWorks
0945	Break
1110	Poster / Demo B: High Performance Software Technologies
1205	Lunch (View Posters)
	Auditorium
1335	Session 4: Award Finalists Session – Advanced Software
1515	Break (View Posters, 25 min.)
1540	Panel: Will Software Save Moore's Law?
1730	Adjourn

0730 **Check-in / Poster Setup / Continental Breakfast**

0830 **Announcements**
Robert Bond / MIT Lincoln Laboratory

0835 **Session 3: Advanced Parallel Environments**
Mike Harris / BAE Systems

0845 **X10 Programming** (Invited)
Vivek Sarkar / IBM Research

0915 **MathWorks Recent and Future Solutions for High Productivity Technical Computing** (Invited)
Roy Lurie / MathWorks
Cleve Moler / MathWorks

0945 **Break (View Posters)**

1000 **Advanced Hardware and Software Technologies for Ultra-long FFT's**
Hahn Kim / MIT Lincoln Laboratory
Jeremy Kepner / MIT Lincoln Laboratory
Michael Vai / MIT Lincoln Laboratory
Crystal Kahn / MIT Lincoln Laboratory

1030 **An Interactive Approach to Parallel Combinatorial Algorithms with Star-P**
John Gilbert / University of California, Santa Barbara
Viral Shah / University of California, Santa Barbara
Todd Letsche / Silicon Graphics, Inc.
Steven Reinhardt / Silicon Graphics, Inc.
* Alan Edelman / MIT

21 September *(Continued)*

1100 **Poster / Demo B: High Performance Software Technologies**
Albert Reuther / MIT Lincoln Laboratory

1110 **Poster / Demo B Précis**

Poster B.1 **Process and Shared Object Library Scheduling for High-Performance Hybrid-Reconfigurable Embedded Systems**
Philip Brisk / UCLA Computer Science Department
Adam Kaplan / UCLA Computer Science Department
Majid Sarrafzadeh / UCLA Computer Science Department

Poster B.2 **Improving Rapid Application Development Environments Through Coordination**
Nicholas Carriero / Yale University
David Gelernter / Yale University
Martin Schultz / Yale University

Poster B.3 **Performance Estimates of a STAP Benchmark on the IBM Cell Processor**
Luke Cico / Mercury Computer Systems, Inc.
Jon Greene / Mercury Computer Systems, Inc.
Robert Cooper / Mercury Computer Systems, Inc.

Poster B.4 **Open HPEC Systems: Design and Profiling Tools for Multiprocessor Signal Processing Applications Using MPI**
Benoît Guillon / Thales Computers
Jérôme Blanc / Thales Computers
Benoît Masson / Thales Computers
Gerard Cristau / Thales Computers
* Vincent Chuffart / Thales Computers

Poster B.5 **Integration of Interactive MATLAB and Linux Clusters**
Joan Puig Giner / Interactive Supercomputing, Inc.
Vern Shrauger / Interactive Supercomputing, Inc.

Poster B.6 **Application of Functional Coverage-Driven-Verification (CDV) Methodology to Real-Time Embedded Systems-on-Chip (SoC) for HW/SW State-Space Co-verification and Architectural Exploration**
Giles Hall / Cadence Design Systems, Inc.
* J. Marc Edwards / Cadence Design Systems, Inc.

Poster B.7 **Combining Moore's Law and Amdahl's Law and Communication: How Software Can Save Moore's Price/Performance Model**
Kevin Howard / Massively Parallel Technologies
James Lupo / Massively Parallel Technologies

Poster B.8 **What Makes HPEC Applications Challenging? – Understanding Application/Architecture Interactions**
David Koester / The MITRE Corporation

Poster B.9 **InfiniPath: A New High Speed, Low Latency Cluster Interconnect**
Greg Lindahl / PathScale, Inc.

Poster B.10 **How Code Generation Will Save Moore's Law**
William Lundgren / Gedae, Inc.
Kerry Barnes / Gedae, Inc.
James Steed / Gedae, Inc.

Poster B.11 **Evaluation of Graphical Programming and Automated Code Generation Software Tools for Use in Missile Defense Applications**
Rick Pancoast / Lockheed Martin MS2
Chris Robbins / Management Communications & Control, Inc.
Rocco Dragone / Lockheed Martin MS2
Joann Harvey / Lockheed Martin MS2
Walter Spehalski / Lockheed Martin MS2

21 September *(Continued)*

Poster B.12 **FPGA Implementation of MIMO Wireless Receiver in Interference**
Tri Phuong / MIT Lincoln Laboratory
Derek Young / MIT Lincoln Laboratory
Daniel Bliss / MIT Lincoln Laboratory
Keith Forsythe / MIT Lincoln Laboratory

Poster B.13 **Applying Model Driven Architecture to Radar Systems**
Terri Potts / Raytheon Company
Stefanie Chiou / Raytheon Company
Gregory Eakman / PathFinder Solutions

Poster B.14 **Scalable and Portable Supercomputing**
Gail Walters / CPU Technology, Inc.
Scott Nelson / CPU Technology, Inc.
Steven Manuel / CPU Technology, Inc.

Poster B.15 **Accelerating Blocked Matrix-Matrix Multiplication Using a Software-Managed Memory Hierarchy with DMA**
Roland Wunderlich / Carnegie Mellon University
Markus Püschel / Carnegie Mellon University
James Hoe / Carnegie Mellon University

1205 **Lunch (View Posters)**

21 September *(Continued)*

1335 **Session 4: Award Finalists Session – Advanced Software**
Rick Pancoast / Lockheed Martin

1345 **pMapper: Automatic Mapping of Parallel Matlab Programs**
Nadya Travinin / MIT Lincoln Laboratory
★ Henry Hoffmann / MIT Lincoln Laboratory
Robert Bond / MIT Lincoln Laboratory
Hector Chan / MIT Lincoln Laboratory
Jeremy Kepner / MIT Lincoln Laboratory
Edmund Wong / MIT Lincoln Laboratory

1415 **VSIPL++Pro – A High-Performance VSIPL++ Implementation**
Jules Bergmann / CodeSourcery, LLC
★ Mark Mitchell / CodeSourcery, LLC
Stefan Seefeld / CodeSourcery, LLC
Zack Weinberg / CodeSourcery, LLC
Nathan Myers / CodeSourcery, LLC
Rick Pancoast / Lockheed Martin, NE&SS

1445 **High-Productivity Stream Programming for High-Performance Systems**
Rodric Rabbah / MIT CSAIL
★ Bill Thies / MIT CSAIL
Michael Gordon / MIT CSAIL
Janis Sermulins / MIT CSAIL
Saman Amarasinghe / MIT CSAIL

1515 **Break (View Posters)**

1540 **Panel: Will Software Save Moore's Law?**
Moderator: Dr. James C. Anderson / MIT Lincoln Laboratory
Distinguished Panelists:
Mr. Robert Bond / MIT Lincoln Laboratory
Dr. Vivek Sarkar / IBM Research
Dr. Guy L. Steele / Sun Microsystems
Dr. William Bail / The MITRE Corporation

1730 **Adjourn**

★ **Denotes outstanding submission**

* **Denotes presenter other than first author**

22 September

Day 3 at a Glance

0730	Check-in / Poster Setup / Continental Breakfast	
0830	Announcements	
0835	Invited Speaker: John Grosh / OSD	
	Auditorium	
0905	Session 5: Standards Usage and Updates	
1010	Break	
1115	Poster / Demo C: Software Standards	
1200	Lunch (View Posters)	
	Auditorium	**S2-180**
1315	Session 6: Advanced Systems	Focus 2: Hardware Tools and Network Technologies
1430	Break (View Posters, 20 min.)	Break (View Posters, 20 min.)
1650	Adjourn / Awards	

0730 **Check-in / Poster Setup / Continental Breakfast**

0830 **Announcements**
Robert Bond / MIT Lincoln Laboratory

0835 **Software Producibility** (Invited)
John Grosh / OSD

0905 **Session 5: Standards Usage and Updates**
Craig Lund / Mercury Computer Systems
Auditorium

0925 **Using the OCP Standard for FPGA Reuse**
Ian Mackintosh / OCPIP

0940 **OMG Data-Distribution Service (DDS): Architectural Update**
Joseph Schlesselman / Real-Time Innovations, Inc.
* Gerardo Pardo-Castellote / Real-Time Innovations, Inc.
Bert Farabaugh / Real-Time Innovations, Inc.

0955 **Eclipse for High-Performance Computing**
Sky Matthews / IBM Rational Software

1010 **Break (View Posters)**

1025 **UML2.0 Profiles for Modeling Real-Time and Quality of Service**
Sky Matthews / IBM Rational Software

1040 **Integrating VSIPL Support in the Dataflow Interchange Format**
Chia-Jui Hsu / University of Maryland at College Park
Shuvra Bhattacharyya / University of Maryland at College Park

1055 **Implementation of an Embedded DoD VSIPL Application on the DARPA Polymorphous Computing Architectures (PCA) RAW Processor**
Joseph Cook / Lockheed Martin MS2
Stephen Crago / University of Southern California, ISI
Lou Morda / Lockheed Martin MS2
Rick Pancoast / Lockheed Martin MS2
Jinwoo Suh / University of Southern California, ISI

22 September *(Continued)*

1115 **Poster / Demo C: Software Standards**
Jeremy Kepner / MIT Lincoln Laboratory

1125 **Poster / Demo C Précis**

Poster C.1 **VSIPL++: A Signal Processing Library Scaling with Moore's Law**
Jules Bergmann / CodeSourcery, LLC
Jeffrey Oldham / CodeSourcery, LLC

Poster C.2 **A Software Methodology for Real-Time Target Recognition**
Wim Bohm / Colorado State University
Steve Heistand / SRC Computers, Inc.
David Caliga / SRC Computers, Inc.
Jeff Hammes / SRC Computers, Inc.

Poster C.3 **An FPGA API for VSIPL++**
Ben Cordes / Northeastern University
* Miriam Leeser / Northeastern University
Joe Tarkoff / Northeastern University

Poster C.4 **Implementation of Floating-Point VSIPL Functions on FPGA-Based Reconfigurable Computers Using High-Level Languages**
Malachy Devlin / Nallatech, Ltd.
Robin Bruce / Institute of System-Level Integration
Stephen Marshall / Strathclyde University

Poster C.5 **Evaluation of an Embedded Signal Processing System for a Generic Air Track Processor**
Robert Hamilton / CSP, Inc.
Stephen Shank / Lockheed Martin Corporation
John Johansson / Lockheed Martin Corporation
Henry Chin / Lockheed Martin Corporation
Rick Pancoast / Lockheed Martin Corporation
Leon Trevito / Lockheed Martin Corporation
Peter Case / Lockheed Martin Corporation
Aubrey Chan / Lockheed Martin Corporation
Juan Antonio Villalba Camacho / Indra
Francisco Alvarez Solvez / Indra
Eva Valentin Ramiro / Indra

Poster C.6 **Return of the Hypercube: 10 Gbps per Node over 802.3ab, Scaling Linearly to 12 Nodes**
Kurt Keville / MIT
Ayodeji Olatunji / Jackson State University

Poster C.7 **FPGA-Based Signal Acquisition System**
Sarah Leeper / Mercury Computer Systems, Inc.
Robert Frisch / Mercury Computer Systems, Inc.
Scott Geaghan / Mercury Computer Systems, Inc.
Scott Tetreault / Mercury Computer Systems, Inc.
Michael Vinskus / Mercury Computer Systems, Inc.
Erich Whitney / Mercury Computer Systems, Inc.

Poster C.8 **The Scalable Software Interconnect for Distributed Radar Signal Processing**
Jeff Rudin / Mercury Computer Systems, Inc.
Luke Cico / Mercury Computer Systems, Inc.
Ken Cain / Mercury Computer Systems, Inc.
Myra Jean Prelle / Mercury Computer Systems, Inc.
Ethan Luce / Raytheon Company
Terri Potts / Raytheon Company

Poster C.9 **A CMOS Digital Decoder ASIC for an Advanced Digital Receiver**
Charles Snell / Lockheed Martin MS2
Leopold Pellon / Lockheed Martin MS2
Junius Pridgen / Lockheed Martin MS2
Melody Jiang / Lockheed Martin MS2
Dipakkumar Tailor / Lockheed Martin MS2
David Lusk / Lockheed Martin MS2

1200 **Lunch (View Posters)**

22 September *(Continued)*

1315 **Session 6: Advanced Systems**
Bill Harrod / SGI
Auditorium

1330 **Adapting Parallel Backprojection to an FPGA Enhanced Distributed Computing Environment**
Albert Conti / Northeastern University
Ben Cordes / Northeastern University
Miriam Leeser / Northeastern University
Eric Miller / Northeastern University
Richard Linderman / AFRL/IF

1400 **An Embedded DoD Discrimination and Classification Processing Challenge for DARPA Architectures for Cognitive Information Processing (ACIP)**
Steve Crago / University of Southern California
Rocco Dragone / Lockheed Martin MS2
* Michael Iaquinto / Lockheed Martin MS2
Jim Kilian / Lockheed Martin MS2
Janice McMahon / University of Southern California
Rick Pancoast / Lockheed Martin MS2

1430 **Break (View Posters)**

1450 **RapidIO-Based Space System Architectures for Synthetic Aperture Radar and Ground Moving Target Indicator**
David Bueno / HCS Research Laboratory, University of Florida
Chris Conger / HCS Research Laboratory, University of Florida
Adam Leko / HCS Research Laboratory, University of Florida
Ian Troxel / HCS Research Laboratory, University of Florida
Alan George / HCS Research Laboratory, University of Florida

1520 **Case Study: Real-Time Demonstration of a Knowledge-Aided STAP Algorithm Using PVL**
Martin Courtney / Information Systems Laboratories, Inc.
John Don Carlos / Information Systems Laboratories, Inc.
Jameson Bergin / Information Systems Laboratories, Inc.

1550 **Performance Analysis of Kernel Benchmarks on Tiled Architectures**
James Lebak / MIT Lincoln Laboratory
Ryan Haney / MIT Lincoln Laboratory
Matt Alexander / MIT Lincoln Laboratory
Hector Chan / MIT Lincoln Laboratory
Edmund Wong / MIT Lincoln Laboratory

1620 **High Performance, Environmentally Adaptive Fault Tolerant Computing (EAFTC)**
John Samson, Jr. / Honeywell, Inc.
Jeremy Ramos / Honeywell, Inc.
Alan George / University of Florida
Minesh Patel / Tandel Systems, LLC
Raphael Some / Jet Propulsion Laboratory

1650 **Adjourn / Awards**
Jeremy Kepner / MIT Lincoln Laboratory

1315 **Focus 2: Hardware Tools and Network Technologies**
Steve Paavola / Analogic
Room S2-180

1330 **C-Based Hardware Design Platform for a Dynamically Reconfigurable Processor**
Phil Mulholland / IPFlex, Inc.
Keisuke Ide / IPFlex, Inc.
* Tomoyoshi Sato / IPFlex, Inc.

1400 **Application Development for Hybrid Pipelined Systems**
Mark Franklin / Washington University in St. Louis
Patrick Crowley / Washington University in St. Louis
* Roger Chamberlain / Washington University in St. Louis
Jeremy Buhler / Washington University in St. Louis
James Buckley / Washington University in St. Louis

1430 **Break (View Posters)**

1450 **A Streaming Virtual Machine for GPUs**
Kenneth Mackenzie / Reservoir Labs, Inc.
Daniel Campbell / Reservoir Labs, Inc.
Peter Szilagyi / Reservoir Labs, Inc.

1520 **An Integrated Photonic Network for Multi-Processor Applications**
Assaf Shacham / Columbia University
Keren Bergman / Columbia University

1550 **A High Performance Programming Model for Large-Scale Molecular Dynamics Calculations on Reconfigurable Supercomputers**
Luis Cordova / University of South Carolina
Melissa Smith / Oak Ridge National Laboratory
Sadaf Alam / Oak Ridge National Laboratory
Jeffrey Vetter / Oak Ridge National Laboratory

1620 **High Performance Computing from a General Formalism: Conformal Computing© Techniques Illustrated with a Quantum Computing Example**
Lenore Mullin /.State University of New York–Albany
James Raynolds / State University of New York–Albany
R.M. Mattheyses / GE Global Research

AGENDA