

## **FPGA Acceleration of Information Management Services**

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Field Programmable Gate Arrays (FPGAs) are widely known for their ability to accelerate “number crunching” applications, such as filtering for signal and image processing. However, this paper reports on the ability of FPGAs to greatly accelerate non-numerical applications, particularly fundamental operations supporting publish—subscribe information management environments. The specific core service accelerated by FPGAs is the brokering of XML metadata of publications against the XPATH logical predicates expressing the types of publications that the subscribers wish to receive. The acceleration is not achieved solely by the FPGA, but by its close coordination with a programmable processor within a Heterogeneous, HPC architecture (HHPC). Two subtasks addressed by the FPGA are the parsing of the ASCII XML publication metadata into an exploitable binary form, followed by the partial evaluation of up to thousands of subscription predicates, with results reported back to the programmable processor.

On the first subtask, the FPGA implements a state machine that parses 1 ASCII character per clock cycle, presently with a 50 MHz clock on 6M gate Xilinx Virtex II FPGAs. This reduces parse time of typical information object metadata from 2 milliseconds to around 50 microseconds (40X speedup). Once the data is parsed, the fields broadcast to parallel logic, which evaluates the subscription predicates. The FPGA synthesis tools do a surprising effective job of optimizing the logic to evaluate these XPATH predicates. In one typical case, 2000 predicates compiled down to only require 2.9% of the 6M gate FPGA resources.

This is ongoing research, the paper will present the latest results which we expect will include results of the FPGA acceleration in the context of the overall information management system and exploration of accelerator performance across critical system parameters including number and diversity of predicates, length and types of fields in the publication metadata, and programmable processor/FPGA interface.