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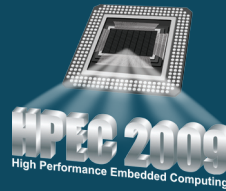Mr. Daniel Wells / The Boeing Company

Thirteenth Annual Workshop on

High Performance Embedded Computing

22–24 September 2009
Massachusetts Institute of Technology
Lincoln Laboratory

Call for Presentations

The High Performance Embedded Computing (HPEC) technical committee announces the Thirteenth Annual HPEC workshop to be held 22–24 September 2009 at MIT Lincoln Laboratory in Lexington, MA. The workshop will give U.S. government-funded researchers from academia, industry and government, working in this important area, an opportunity to discuss techniques, approaches and ongoing developments with relevance to real-time embedded computing and related military applications. During this thirteenth year, the HPEC 2009 Workshop will have as its theme "Diversified and heterogeneous computing architectures and their impact on DoD HPEC systems." The technical committee seeks new presentations that clearly describe advances in high performance embedded computing technologies, emphasizing one or more of the following topics:

- Advanced Multicore Software Technology
- Automated Design Tools
- Mapping and Scheduling of Parallel and Real-Time Applications
- Case Studies and Benchmarking of HPEC Applications
- Signal Processing Techniques
- Computing Technologies for Challenging Form Factors
- ASIC and FPGA Advances
- Parallel and Open System Architectures
- Networking and Interconnects
- Fault-Tolerant Computing
- Digital Front-Ends
- Advanced Codesign Techniques
- Advanced Processor Architectures

All submittals will be competitively reviewed and judged on their technical merit, novelty and relevance to the technical program. Preference will be given to papers with strong, quantitative results. The workshop will have both Open Sessions and Unclassified/U.S. Only sessions, as well as poster presentations. Presenters with significant hardware demonstrations are encouraged to apply to the poster sessions. Since the presentations themselves will constitute the published proceedings, speakers are requested to prepare charts of the highest quality. Electronic copies of the charts presented at the workshop will be included in the workshop proceedings.

Authors are invited to submit two-page extended abstracts via our web site:

http://www.ll.mit.edu/HPEC

For further details about the workshop, please contact

HPEC Workshop Office
Joan Napoli, Supervisor
Lori Tsoulas, Workshop Administrator
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Important Dates: Abstract submission deadline   21 May 2009
                   Notification of acceptances   26 June 2009

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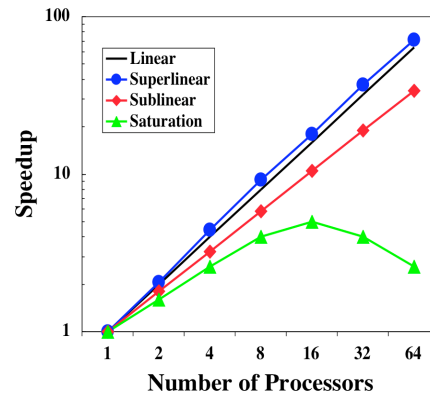**Figure 1: Conceptual diagram of system.**

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Example of a Chart

Figure 2: Performance results.

References

References should be listed in the format shown below with numbering in square brackets. References ("Reference" style) should be set at Times 9 pt font and fully justified within the column.

[1] I. Foster and C. Kesselman, *The Grid: Blueprint for a New Computing Infrastructure*, Second Edition, Morgan-Kaufman, 2004.

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